TD25C128-H

128-Kbit SPI Serial EEPROM

DATASHEET Rev.1.1

Features

- Serial Peripheral Interface (SPI) Compatible
  - SPI Modes 0 (0, 0) and 3 (1, 1) supported
- Supply Voltage Range: 1.7V to 5.5V
- High Speed Clock: 20 MHz
- Byte and Page (up to 64 Bytes) Write Mode
- Self-timed Write Cycle (3ms Maximum)
- Block Write Protection
  - Quarter, Half or Whole Memory Array
- Additional 64-byte Write Lockable Page and 128-bit Unique ID
- Ultra High Reliability
  - Endurance: 6,000,000 Write Cycles
  - Data Retention: 300 Years
  - ESD Protection (Human Body Model): 6000V
- Operating Temperature Range: -40°C to +105°C
- Green Packaging Options (RoHS Compliant, Pb/Halogen-free)
  - SOP, TSSOP, UDFN

Description

The TD25C128-H is a serial EEPROM device accessed through the SPI bus. The device is designed to operate in a supply voltage range of 1.7V to 5.5V, with a maximum of 20 MHz transfer rate. The operating temperature range is from -40°C to +105°C.

The serial EEPROM memory is organized as 256 pages of 64 bytes each, totaling 16384*8 bits. The device offers an additional 64-byte Identification Page for users to store sensitive application parameters. This page can be permanently locked in Read-only mode after the application data is written into the Identification Page. The device also offers a separate memory block containing a factory programmed 128-bit Unique ID. This block is in Read-only mode and can be accessed to by sending a specific Read command.

The TD25C128-H is delivered in lead-free green packages: SOP, TSSOP and UDFN.

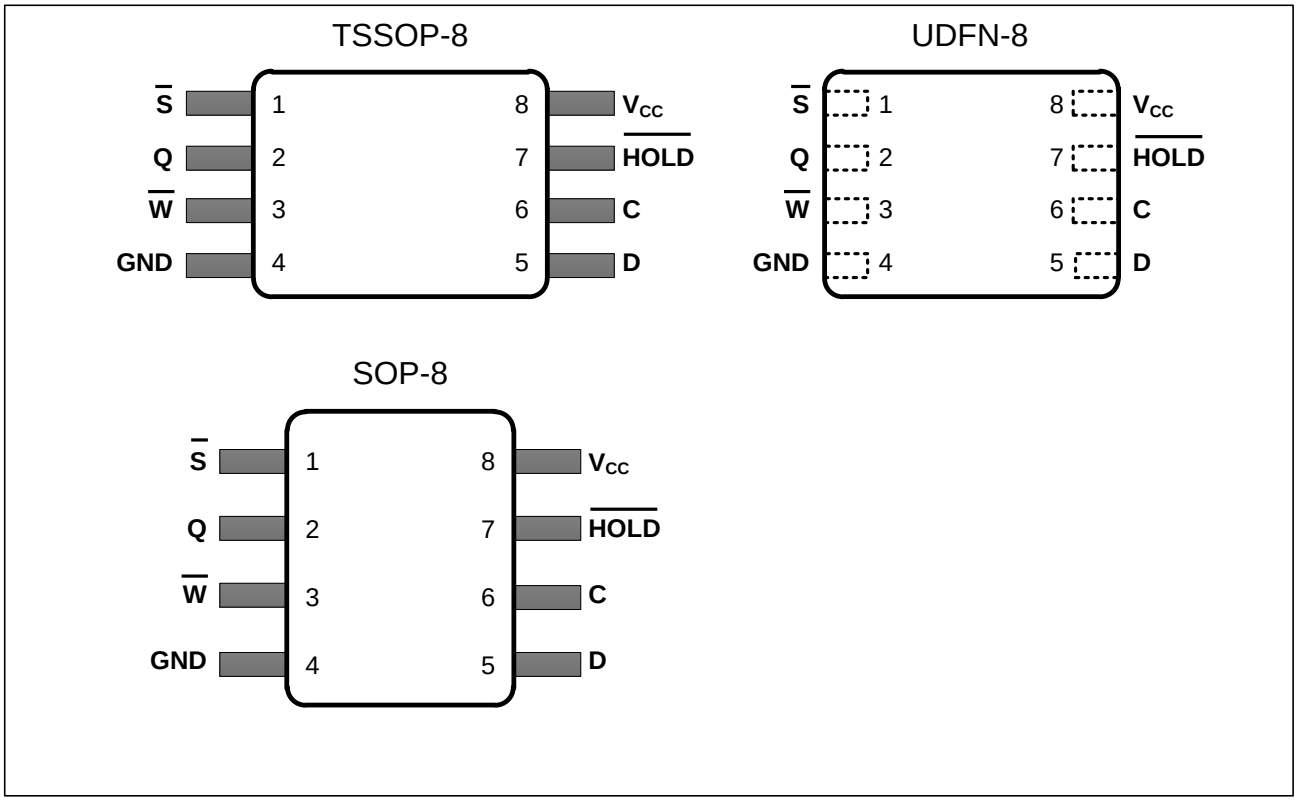
Table of Contents

1 Pin Descriptions and Pin Configuration

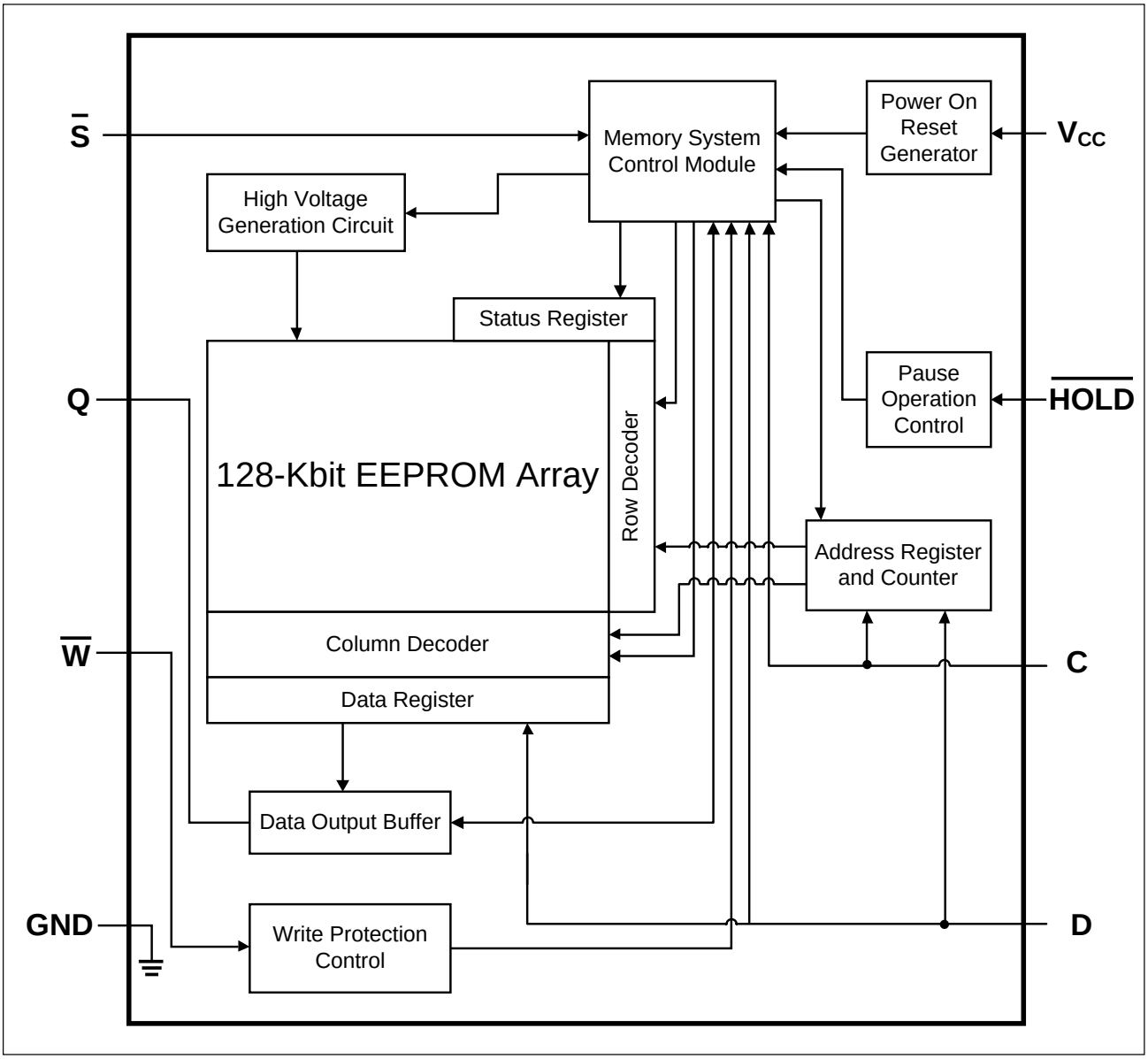
Table 1–1 Pin Descriptions

Symbol	Type	Name and Function
C	Input	**Serial Clock:** This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) change from the falling edge of Serial Clock (C).
D	Input	**Serial Data Input:** This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values latched on the rising edge of Serial Clock (C).
Q	Output	**Serial Data Output:** This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).
$\overline{S}$	Input	**Chip Select:** When this input signal is high, the device is deselected and Serial Data Output (Q) is at high impedance. The device is in the Standby mode, unless an internal Write cycle is in progress. Driving Chip Select ($\overline{S}$) low selects the device, placing it in the Active mode. After power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.
$\overline{W}$	Input	**Write Protect:** This input pin is used to freeze the size of the area of memory that is protected against write instructions. This pin must be driven either high or low, and must be stable during all Write instructions.
$\overline{HOLD}$	Input	**Hold:** This input signal is used to pause any serial communications with the device without deselecting the device. During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care. To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven low.
V_{CC}	Power	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.
GND	Ground	**Ground:** The ground reference for the device power supply (V_{CC}). GND should be connected to the system ground.

Figure 1–1 Pin Configuration (Top View)



2 Functional Block Diagram



3 Device Communication

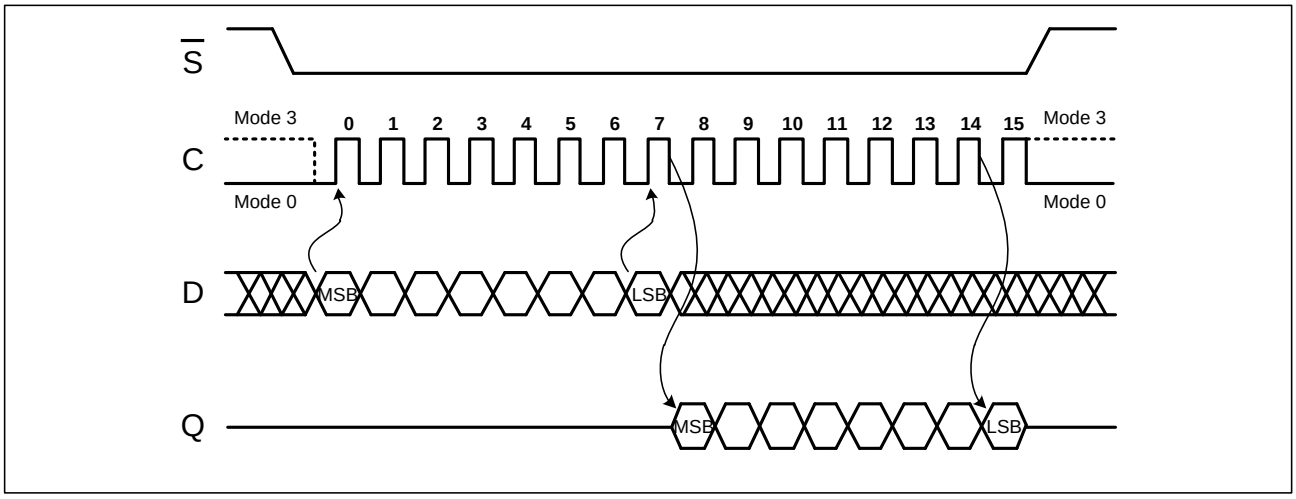
3.1 SPI Mode

The TD25C128-H is controlled by a set of instructions sent from a microcontroller, commonly referred to as the SPI Master. The SPI Master communicates with the device via the SPI bus which is comprised of four signal lines: Chip Select ($\overline{S}$), Serial Clock (C), Serial Data Input (D) and Serial Data Output (Q).

The SPI protocol defines a total of four modes of operation (Mode 0, 1, 2 or 3) with each mode differing in respect to Serial Clock (C) polarity (CPOL) and phase (CPHA) and how the polarity and phase control the flow of data on the SPI bus. The TD25C128-H supports two most common modes: SPI Mode 0 (CPOL=0, CPHA=0) and Mode 3 (CPOL=1, CPHA=1). For SPI Modes 0 and 3, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes is the clock polarity when the bus Master is in Standby mode and not transferring data (see **Figure 3–1**).

Figure 3–1 SPI Mode 0 and Mode 3



3.2 SPI Bus Connection

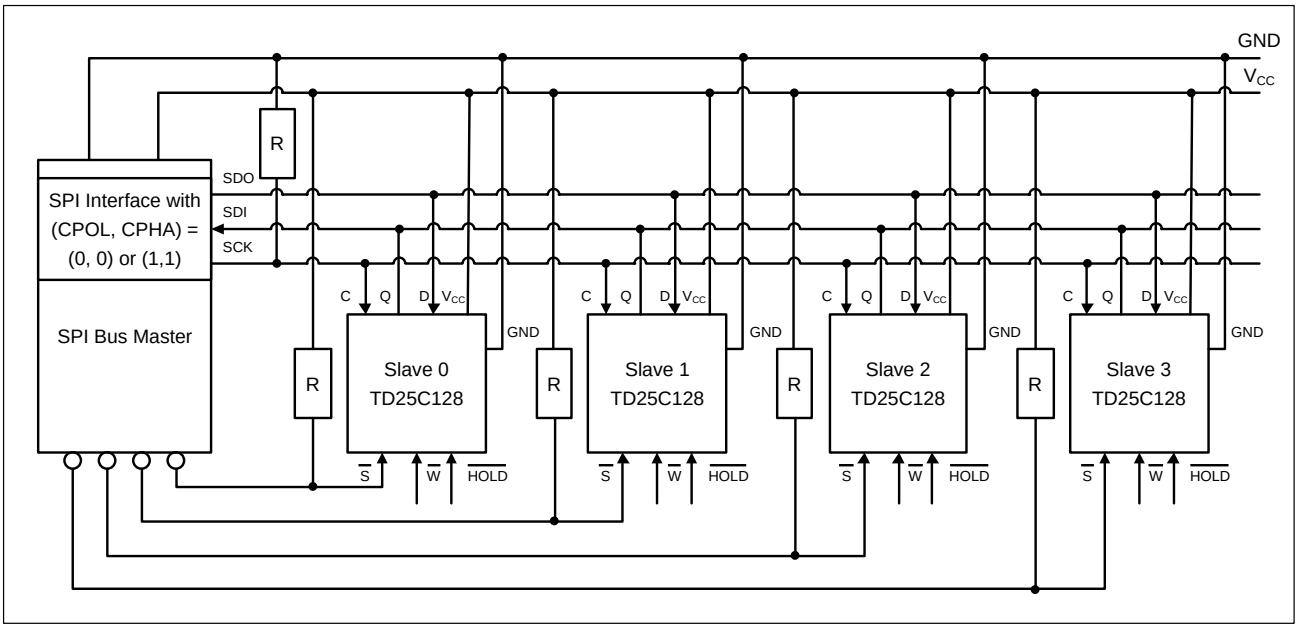
All instructions, addresses and input data bytes are shifted in to the device with most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of Serial Clock (C) after Chip Select ($\overline{S}$) is driven low.

All output data bytes are shifted out of the device with most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of Serial Clock (C) after an instruction has been clocked into the device.

Figure 3–2 shows an example of four memory devices connected to a SPI bus Master. Only one memory device is selected at a time, so only one memory device drives the Serial Data Output (Q) line at a time. The outputs of other memory devices are high impedance.

The pull-up resistor R ensures that a device is not selected if the bus Master leaves Chip Select ($\overline{S}$) line in the high impedance state.

Figure 3–2 Bus Master and Memory Devices on SPI Bus



3.3 Active and Standby Mode

When Chip Select ($\overline{S}$) is low, the TD25C128-H is selected, and in the Active mode. The device consumes I_{CC}, as specified in DC characteristics (see **Section 5.2**).

When Chip Select ($\overline{S}$) is high, the TD25C128-H is deselected. If an internal write cycle is not currently in progress, the device then goes into the low-power Standby mode.

3.4 Device Reset and Initialization

The TD25C128-H incorporates a Power-On Reset (POR) circuit to prevent inadvertent operations during power-up. On a cold power-up, the device does not respond to any instructions until the supply voltage reaches the internal power-on reset threshold voltage (V_{POR}). The supply voltage must rise continuously between V_{POR} and V_{CC}(Min). During this time, the Chip Select ($\overline{S}$) line is not allowed to float but should follow the V_{CC}. Therefore, it is recommended to connect the Chip Select ($\overline{S}$) line to V_{CC} via a pull-up resistor. Once the supply voltage passes V_{POR}, the device is reset and enters Standby mode. However, no protocol should be issued to the device until a valid and stable supply voltage is applied for the time specified by the t_{INIT}. The supply voltage must remain stable and valid until the end of the protocol transmission, and for a write instruction, until the end of the internal write cycle (see **Figure 3–3**).

This POR behavior is bi-directional. It protects the TD25C128-H against brown-out failure caused by a temporary loss of power. In a similar way, as soon as the supply voltage drops below the internal brown-out reset threshold voltage (V_{BOR}), the device is reset and stops responding to any instructions (see **Figure 3–3**). The V_{BOR} level is set below the V_{POR} level.

Parameters related to power-up and power-down conditions are listed in **Table 3–1**.

Figure 3–3 Power-up and Power-down Timing

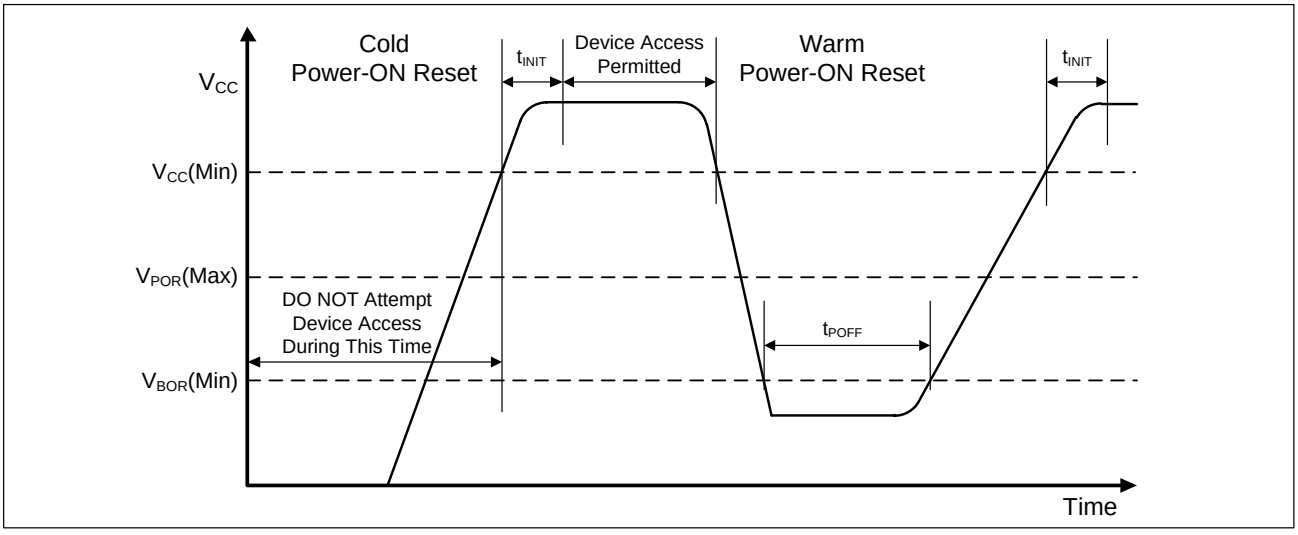


Table 3–1 Power-up and Power-down Conditions

Symbol	Parameter	Min	Max	Unit
V_{POR}	Power-On Reset Voltage	-	1.5	V
V_{BOR}	Brown-out Reset Voltage	1.2	-	V
t_{INIT}	Time from V_{CC}(Min) to First Command	100	-	μs
t_{POFF}	Warm Power Cycle Off Time	100	-	μs

3.5 Hold Conditon

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, the Hold condition has no effect on the internal write cycle. Therefore, if a write cycle is in progress, driving the Hold ($\overline{HOLD}$) signal low will not pause the operation and the write cycle will continue to completion.

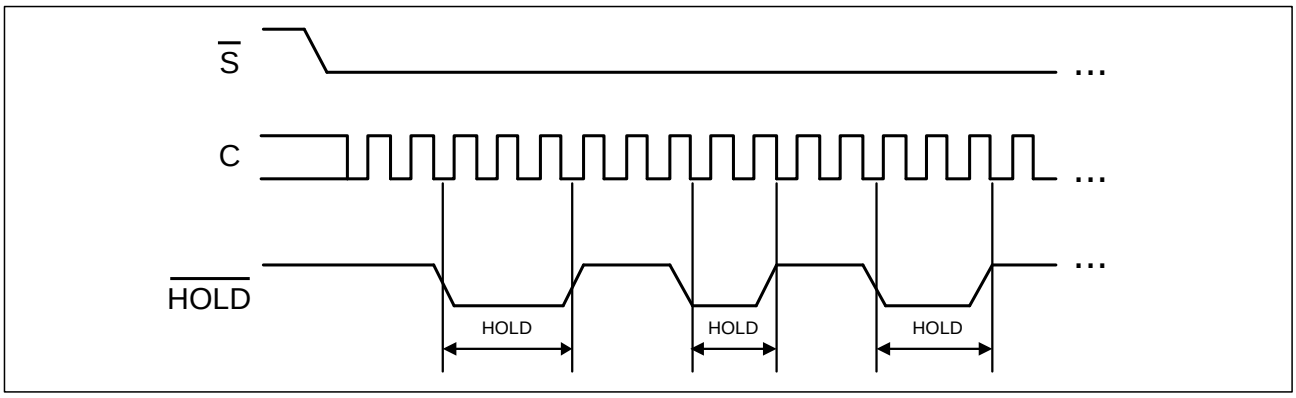
To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) low. The Hold condition starts when the Hold ($\overline{HOLD}$) signal is driven low while the Serial Clock (C) is already low. If the Hold ($\overline{HOLD}$) signal is driven low during the Serial Clock (C) high pulse, then the Hold condition will not be started until the beginning of the next Serial Clock (C) low pulse.

During the Hold condition, the Serial Data Output (Q) is high impedance, and the Serial Data Input (D) and the Serial Clock (C) are Don't Care.

To end the Hold condition, the Hold ($\overline{HOLD}$) signal is driven high when the Serial Clock (C) is low. If the Hold ($\overline{HOLD}$) signal is driven high during the Serial Clock (C) high pulse, then the Hold condition will not end until the beginning of the next Serial Clock (C) low pulse (see **Figure 3–4**).

Normally, the device is kept selected for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition has the effect of resetting the state of the device.

Figure 3–4 Hold Condition Activation



3.6 Data Protecion

The TD25C128-H features the following data protection mechanisms:

- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit (see **Section 4.2** for details).
- The Block Protect (BP1, BP0) bits in the Status Register are used to configure part of the memory as Read-only (see **Section 4.4.1** for details).
- The Write Protect ($\overline{W}$) signal in accordance with the Status Register Write Protect (SRWR) bit in the Status Register is used to write protect the Status Register (see **Section 4.4.2** for details).

4 Instructions

Each command is composed of bytes with Most Significant Bit (MSB) transmitted first, initiated with an instruction byte, as shown in **Table 4–1**, and starts with a high-to-low Chip Select ($\overline{S}$) transition.

If an invalid instruction is sent (one not contained in **Table 4–1**), the device automatically enters a Wait state until deselected.

Table 4–1 Instruction Set for the TD25C128-H

Instruction Name	Operation Description	Instruction Format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from 128-Kbit Memory Array	0000 0011
WRITE	Write to 128-Kbit Memory Array	0000 0010
RDID	Read Identification Page	1000 0011
WRID	Write Identification Page	1000 0010
RDLS	Read Identification Page Lock Status	1000 0011
LID	Lock Identification Page in Read-only Mode	1000 0010
RDUID	Read Unique ID	1000 0001

4.1 Read Status Register (RDSR)

The TD25C128-H includes an 8-bit Status Register. The Status Register bits modulate various features of the device as shown in **Table 4–2**.

Table 4–2 Status Register Bit Definition and Function

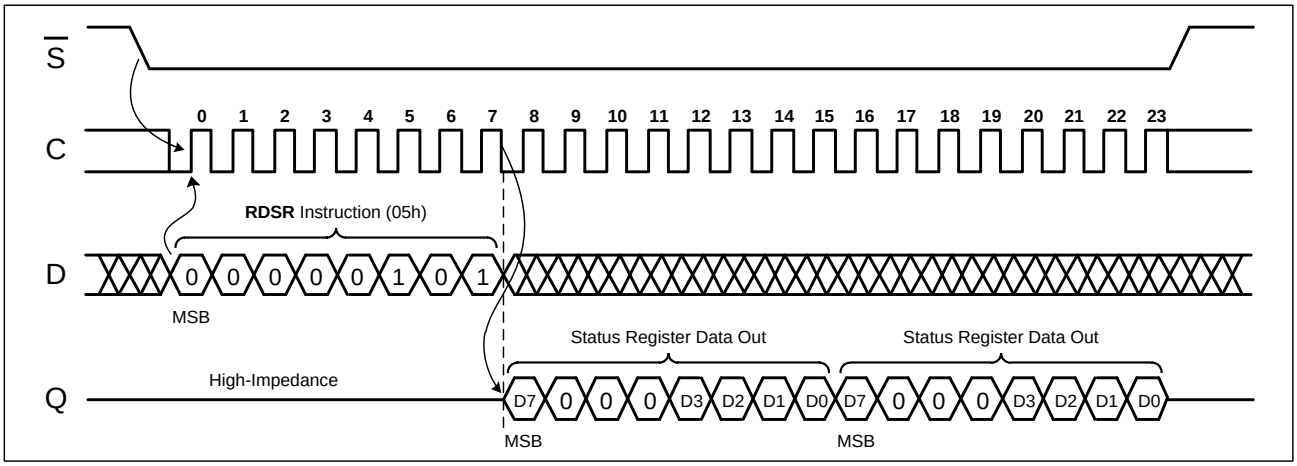
Bit	Name	Function	Description	
7	SRWD	Status Register Write Protect	0	Write Protect ($\overline{W}$) pin is not enabled (Initial Delivery State)
			1	Write Protect ($\overline{W}$) pin is enabled (see **section 4.4.2** for detail)
6:4	RFU	Reserved for Future Use	0	Read always as '000'
3	BP1	Block Protect	00	No memory array write protection (Initial Delivery State)
			01	Quarter memory array write protection (see **section 4.4.1** for detail)
2	BP0		10	Half memory array write protection (see **section 4.4.1** for detail)
			11	Whole memory array write protection (see **section 4.4.1** for detail)
1	WEL	Write Enable Latch	0	Device is not write enabled (Power-up state)
			1	Device is write enabled
0	WIP	Write In Progress	0	No write cycle is in progress, device is ready for new instruction
			1	Device is busy with an internal write cycle

The Read Status Register (RDSR) instruction is used to read the Status Register. This instruction is defined with Chip Select ($\overline{S}$) signal first driven low; the bits of the instruction byte (05h) are then shifted in on Serial Data Input (D). The device will return 8-bit Status Register value on Serial Data Output (Q). If Chip Select ($\overline{S}$) continues to be driven low, the Status Register value is shifted out continuously (see **Figure 4–1**).

The RDSR instruction is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of Chip Select ($\overline{S}$) can occur at any time during the cycle.

The Status Register can be read at any time, even while an internal write cycle is in progress. When a write cycle is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device.

Figure 4–1 Read Status Register

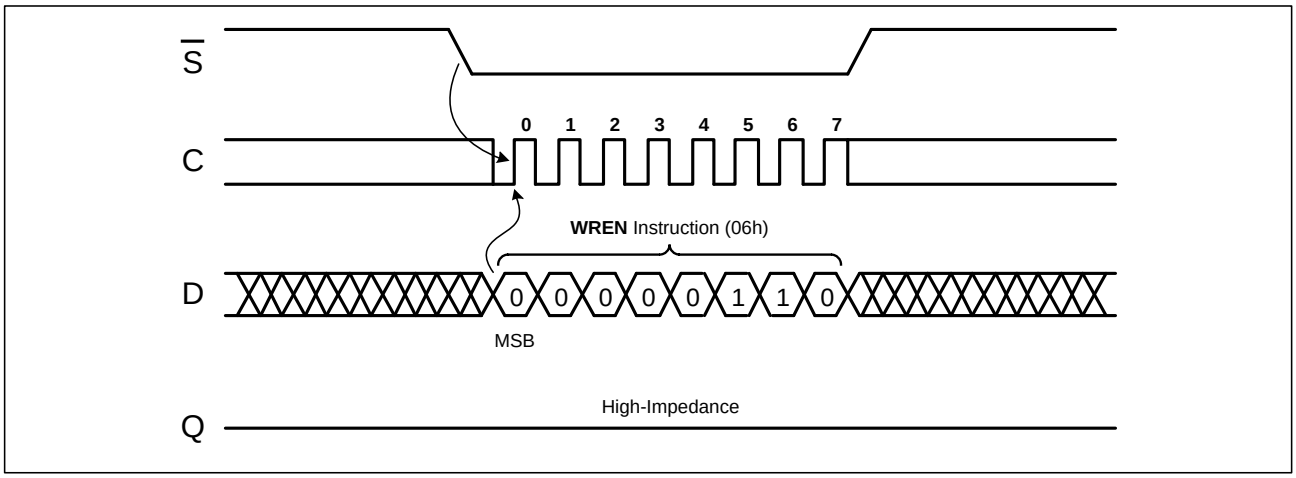


4.2 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable (WREN) instruction to the device.

To send WREN instruction to the device, Chip Select ($\overline{S}$) is first driven low, and the bits of the instruction byte (06h) are shifted in, on Serial Data Input (D) (see **Figure 4–2**). The device then enters a Wait state. It waits for the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

Figure 4–2 Write Enable



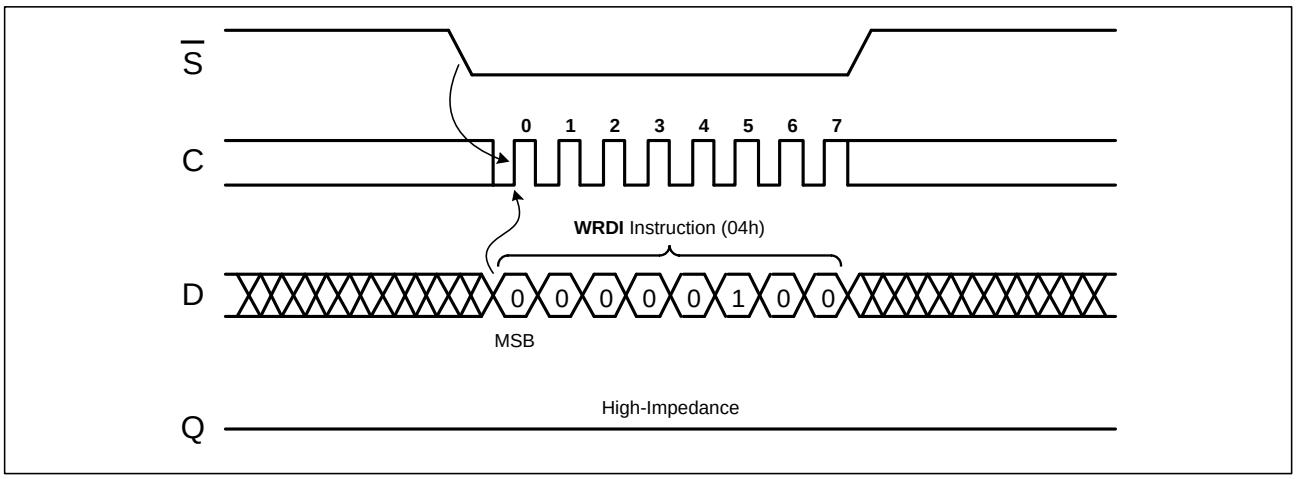
4.3 Write Disable (WRDI)

One way of resetting the WEL bit is to send a Write Disable (WRDI) instruction to the device. To send a WRDI instruction to the device, Chip Select ($\overline{S}$) is first driven low, and the bits of the instruction byte (04h) are shifted in, on Serial Data Input (D) (see **Figure 4–3**). The device then enters a Wait state. It waits for the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

The WEL bit is reset by any of the following events:

- Power-up;
- WRDI instruction execution;
- WRSR or WRITE (including WRID and LID) instruction completion.

Figure 4–3 Write Disable



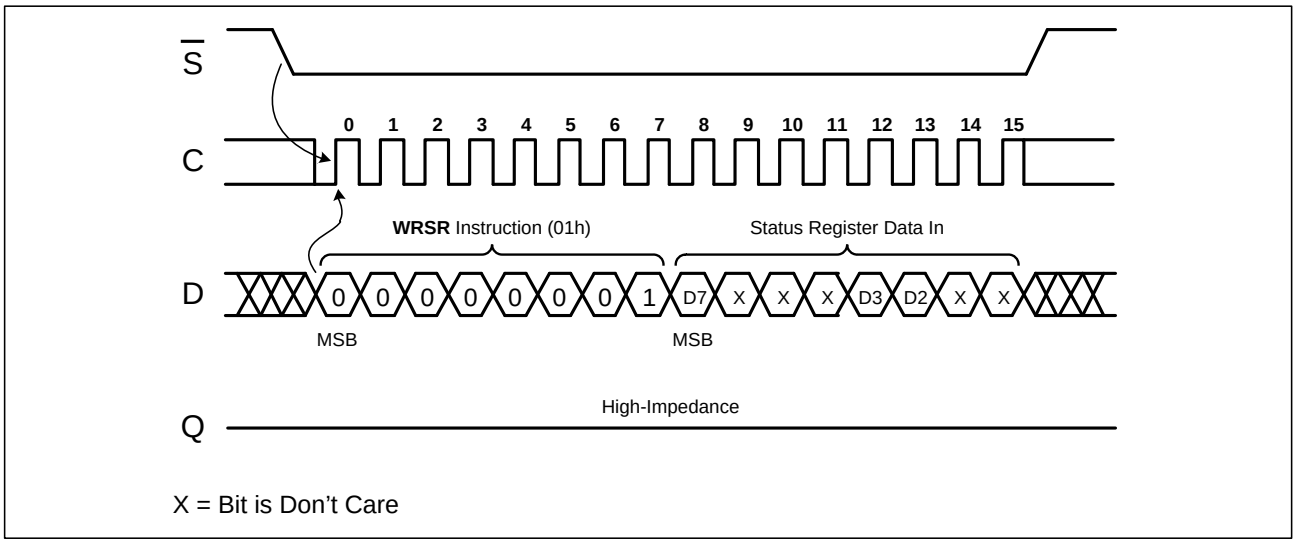
4.4 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction enables the SPI Master to change selected bits of the Status Register. Before a WRSR instruction can be initiated, a WREN instruction must be executed to set the WEL bit to Logic '1'. The WRSR instruction is achieved by driving Chip Select ($\overline{S}$) low, followed by the instruction byte (01h) and the data byte on Serial Data input (D), and then Chip Select ($\overline{S}$) driven high. Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte and before the next rising edge of Serial Clock (C) (see **Figure 4–4**). Otherwise, the WRSR instruction will not be executed.

Driving Chip Select ($\overline{S}$) signal high at a byte boundary of the input data triggers the self-timed write cycle that takes a fix time by the t_{WC} specification to complete. While the write cycle is in progress, the Status Register can still be read to check the value of the WIP bit: the WIP bit is Logic '1' during the self-timed write cycle and is Logic '0' when the write cycle is complete. The WEL bit is also reset at the end of the write cycle.

The WRSR instruction has no effect on the bit 6, bit 5, bit 4, bit 1 and bit 0 in the Status Register, but only enables the user to change the values of the SRWD, BP1 and BP0 bits. These three bits are non-volatile bits that have the same properties and functions as regular EEPROM cells.

Figure 4–4 Write Status Register



4.4.1 Block Write Protection

The WRSR instruction allows the user to selectively write-protect the memory array by blocks through changing the Block Protect bits (BP1, BP0). The Write-Protected Block size and the corresponding Status Register control bits are shown in **Table 4–3**.

Table 4–3 Write-Protected Block Size

Status Register Bits		Protected Block	Protected Address Range
BP1	BP0		TD25C128-H
0	0	None	None
0	1	Upper Quarter	3000h to 3FFFh
1	0	Upper Half	2000h to 3FFFh
1	1	Whole Memory	0000h to 3FFFh

4.4.2 Status Register Write Protection

The WRSR instruction allows the user to set or reset the Write Protection mode of the Status Register itself through changing the Status Register Write Protect (SRWD) bit in accordance with the state of Write Protect ($\overline{W}$) pin.

When the SRWD bit is Logic '0', it is possible to write to the Status Register (provided that the WEL bit has previously been set by a WREN instruction), regardless of the state of Write Protect ($\overline{W}$) pin. When the SRWD bit is set to Logic '1', two cases depending on the state of the Write Protect ($\overline{W}$) pin:

- If Write Protect ($\overline{W}$) is driven high, it is possible to write to the Status Register (provided that the WEL bit has previously been set by a WREN instruction).
- If Write Protect ($\overline{W}$) is driven low, it is not possible to write to the Status Register even if the WEL bit has previously been set by a WREN instruction. As a result, all the data bytes in the memory area, which are write-protected by the Block Protect (BP1, BP0) bits in the Status Register, are also Hardware-protected against data modification.

Regardless of the order of the two cases, the Hardware-protected mode can be entered by: either setting the SRWD bit after driving the Write Protect ($\overline{W}$) pin low, or driving the Write Protect ($\overline{W}$) pin low after setting the SRWD bit. Once the Hardware-protected mode has been entered, the only way of exiting it is to pull high the Write Protect ($\overline{W}$) pin. If the Write Protect ($\overline{W}$) pin has been permanently tied high, the Hardware-protected mode can never be activated.

The protection features of the device are summarized in **Table 4–4**.

Table 4–4 SRWD Protection Modes

SRWD bit	$\overline{W}$ Pin	WEL bit	Status Register	Protected Block	Unprotected Block
0	X	0	Protected	Protected	Protected
0	X	1	Writable	Protected	Writable
1	LOW	0	Protected	Protected	Protected
1	LOW	1	Protected	Protected	Writable
X	HIGH	0	Protected	Protected	Protected
X	HIGH	1	Writable	Protected	Writable

Note: X = Don't Care State.

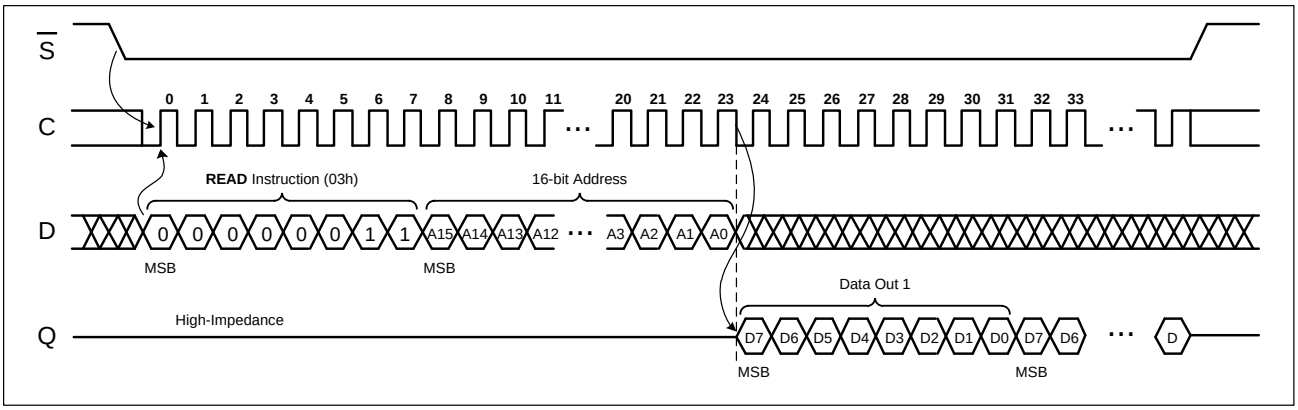
4.5 Read from Memory Array (READ)

Reading the TD25C128-H memory array is achieved with the Read from Memory Array (READ) instruction. To send the READ instruction, Chip Select ($\overline{S}$) signal is first driven low; the bits of the instruction byte (03h) and two address bytes are then shifted in, on Serial Data Input (D). For the 128-Kbit memory array, address bits A13:A0 are significant address bits and A15:A14 are Don't Care bits. The address is loaded into an internal address counter, and the byte of data at the address is shifted out, on Serial Data Output (Q). If Chip Select ($\overline{S}$) continues to be driven low, the address counter is incremented automatically, and the byte of data at the new address is shifted out (see **Figure 4–5**). When the highest address is reached, the address counter will rollover to the lowest address, allowing the read cycle to be continued. Therefore, the whole memory can be read with a single READ instruction.

The read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of Chip Select ($\overline{S}$) can occur at any time during the cycle.

The READ instruction is not accepted, and is not executed, if a write cycle is currently in progress.

Figure 4–5 Read from Memory Array



4.6 Write to Memory Array (WRITE)

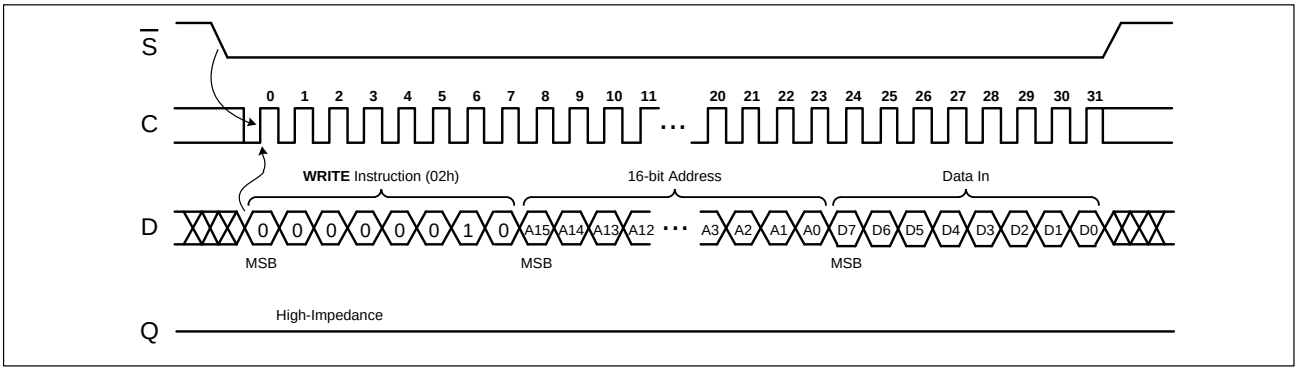
In order to program the TD25C128-H 128-Kbit memory array, two separate instructions must be executed. First, a WREN instruction must be executed to set the device to be write enable. Then, one of the two possible write sequences described below may be executed. The device will ignore the WRITE instruction if the device is not write enable, and return to the Standby mode when Chip Select ($\overline{S}$) is driven high.

4.6.1 Byte Write

A byte write instruction is issued by driving Chip Select ($\overline{S}$) low first, sending the WRITE instruction (02h), the address bytes and a data byte on Serial Data Input (D), and then driving Chip Select ($\overline{S}$) high. For the 128-Kbit memory array, address bits A13:A0 are significant address bits and A15:A14 are Don't Care bits. Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C) (see **Figure 4–6**).

If the addressed page is not in the region protected by the Block Protect (BP1, BP0) bits, driving Chip Select ($\overline{S}$) high at a byte boundary of the input data triggers the self-timed write cycle, which continues for a fix time by the t_{WC} specification. The TD25C128-H will automatically return to the Write Disable state (WEL = 0) at the completion of a write cycle.

Figure 4–6 Byte Write



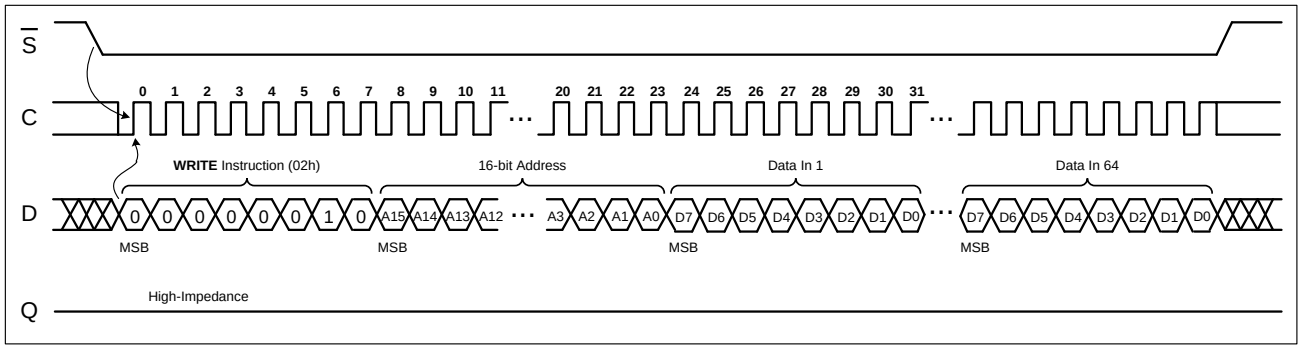
4.6.2 Page Write

A page write sequence allows up to 64 bytes to be written in the same write cycle, provided that all bytes are in the same page of the memory array. Partial page write of less than 64 bytes is allowed. This is achieved by Chip Select ($\overline{S}$) continuing to be driven low after the receipt of each data byte, and the next byte of input data is shifted in (see **Figure 4–7**).

Each time a new data byte is shifted in, the six least significant bits of the internal address counter are incremented. The higher address bits are not incremented and retain the page location. When the internal address reaches the page boundary, a condition known as "roll-over" occurs and the following data byte is placed at the beginning of the same page. In case of roll-over, if more than 64 bytes that exceeding the page size are sent to the device, the previous data will be overwritten.

If the addressed page is not in the region protected by the Block Protect (BP1, BP0) bits, driving Chip Select ($\overline{S}$) high at a byte boundary of the input data triggers the self-timed write cycle, which continues for a fix time by the t_{WC} specification. The TD25C128-H will automatically return to the Write Disable state (WEL = 0) at the completion of a write cycle.

Figure 4–7 Page Write



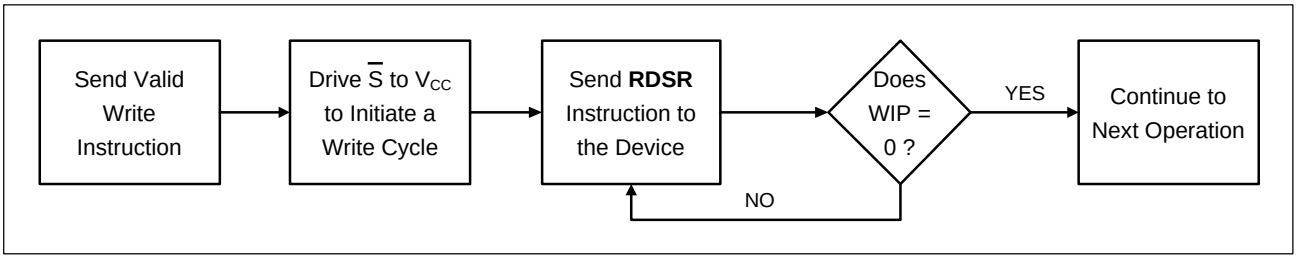
4.6.3 Polling Routine

A polling routine can be implemented to optimize time-sensitive applications that would not prefer to wait the fixed maximum write cycle time (t_{WC}). This method allows the application to know immediately when the write cycle has completed to start a subsequent operation.

Once the internal write cycle has started, a polling routine can be initiated. This involves repeatedly sending RDSR instruction to determine if the device has completed its self-timed write cycle. If the WIP bit (bit 0 of the Status Register) = 1, the write cycle is still in progress; if the WIP bit = 0, the write cycle has ended. If the WIP bit = 1, repeated RDSR commands can be executed until the WIP bit = 0, indicating that the device is ready to execute a new instruction (see **Figure 4–8**).

Only the RDSR instruction is enabled during the write cycle.

Figure 4–8 Polling Flow Chart



4.7 Read Identification Page (RDID)

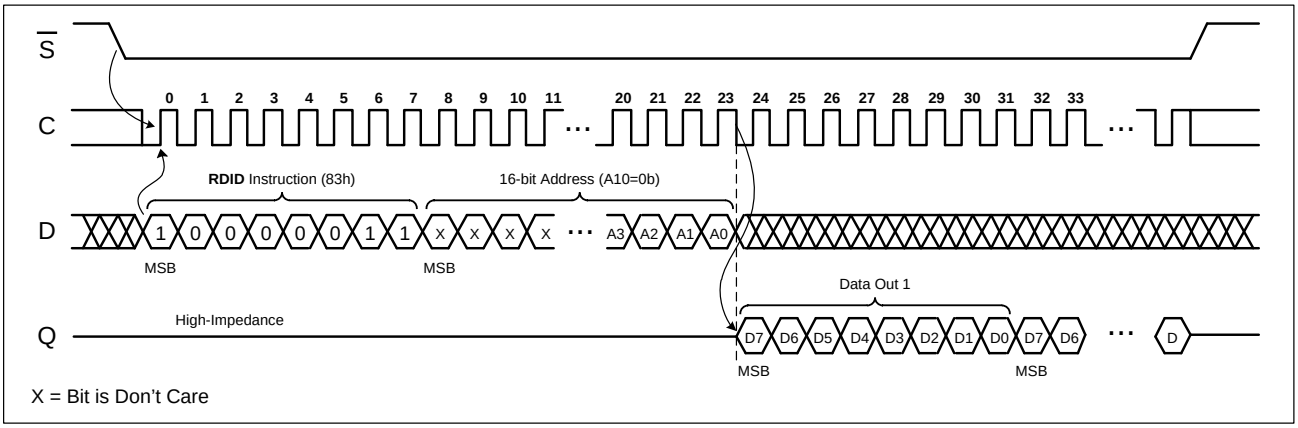
The TD25C128-H offers a 64-byte Identification Page (ID Page) in addition to the 128-Kbit memory array for storage of specific application data. This Identification Page can be written and (later) permanently locked in Read-only mode.

Reading the ID Page is achieved with the Read Identification Page (RDID) instruction. Chip Select ($\overline{S}$) signal is first driven low; the bits of the instruction byte (83h) and the address bytes are then shifted in, on Serial Data Input (D). Address bit A10 must be '0'. Other upper address bits are Don't Care, and the lower address bits A5:A0 define the byte locations inside the Identification Page. The byte of data at this address is shifted out on Serial Data Output (Q). If Chip Select ($\overline{S}$) continues to be driven low, the internal address counter is automatically incremented, and the byte of data at the new address is shifted out (see **Figure 4–9**). When the end of the ID Page is reached, the address counter will rollover to the beginning of the ID Page, allowing the read cycle to be continued.

The read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of Chip Select ($\overline{S}$) can occur at any time during the cycle.

The RDID instruction is not accepted, and is not executed, if a write cycle is currently in progress.

Figure 4–9 Read Identification Page

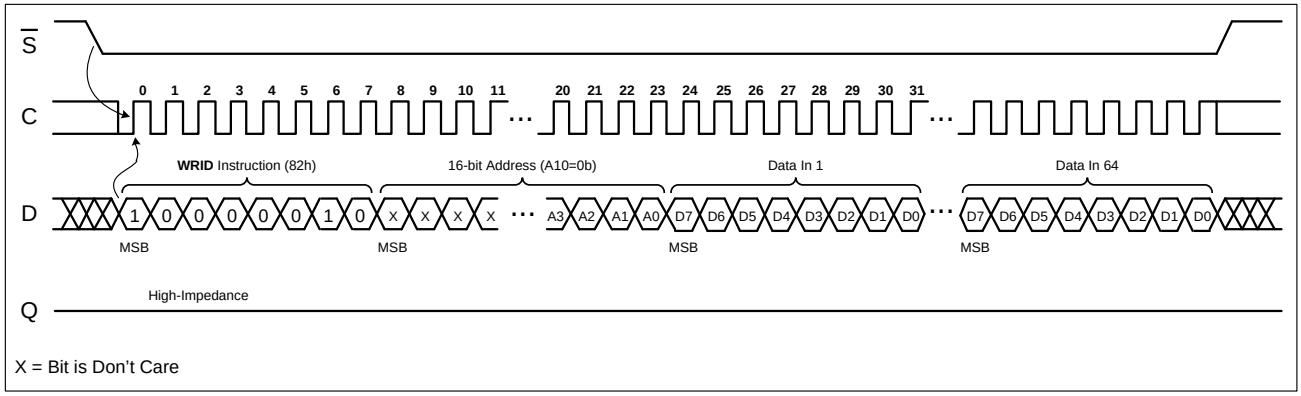


4.8 Write Identification Page (WRID)

Writing the Identification Page is achieved with the Write Identification Page (WRID) instruction. Before this instruction can be accepted, a WREN instruction must have been executed.

The WRID instruction is defined with Chip Select ($\overline{S}$) signal first driven low. The bits of the instruction byte (82h), address bytes, and at least one data byte are then shifted in on Serial Data Input (D). Address bit A10 must be 0. Upper address bits are Don't Care, and the lower address bits A5:A0 address bits define the byte address inside the Identification Page. The instruction is terminated by driving Chip Select ($\overline{S}$) high at a byte boundary of the input data (see **Figure 4–10**). If the Identification Page has not been locked in Read-only mode, the Chip Select ($\overline{S}$) rising edge triggers the self-timed write cycle, which continues for a period of t_{WC}.

Figure 4–10 Write Identification Page



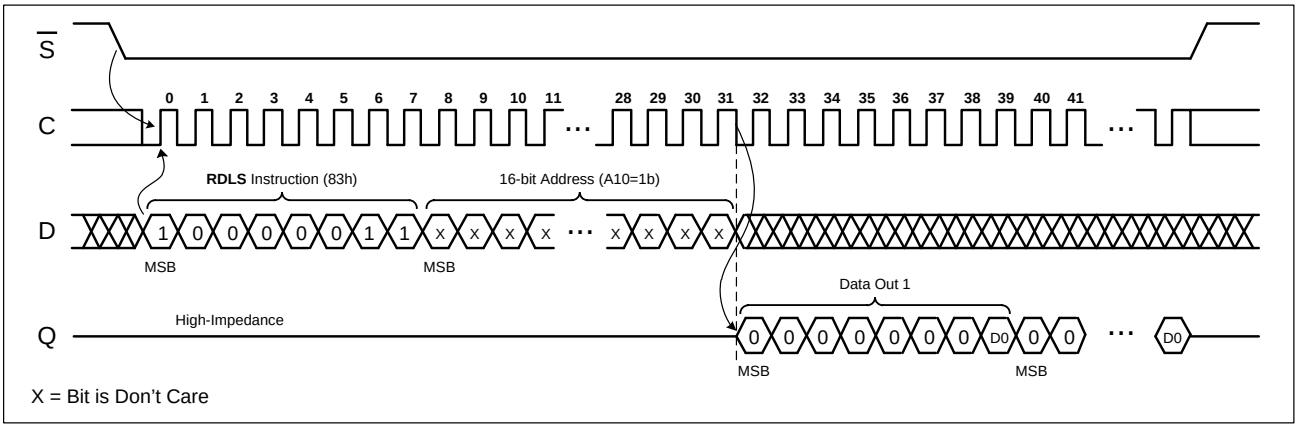
4.9 Read Lock Status (RDLS)

The Read Lock Status (RDLS) instruction is used to check whether the Identification Page is locked in Read-only mode or not. The RDLS instruction is defined with Chip Select ($\overline{S}$) first driven low. The bits of the instruction byte (83h) and the address bytes are then shifted in, on Serial Data Input (D). Address bit A10 must be '1' and all other address bits are Don't Care. The Lock Status bit is the LSB (least significant bit) of the byte read on Serial Data Output (Q). It is Logic '1' when the lock is active and is Logic '0' when the lock is not active. All other bits are always read as '0' (see **Figure 4–11**). If Chip Select ($\overline{S}$) continues to be driven low, the same data byte is shifted out.

The read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of Chip Select ($\overline{S}$) can occur at any time during the cycle.

The RDLS instruction is not accepted, and is not executed, if a write cycle is currently in progress.

Figure 4–11 Read Lock Status



4.10 Lock Identification Page (LID)

The Lock ID (LID) instruction permanently locks the Identification Page in Read-only mode. Before this instruction can be accepted, a WREN instruction must have been executed.

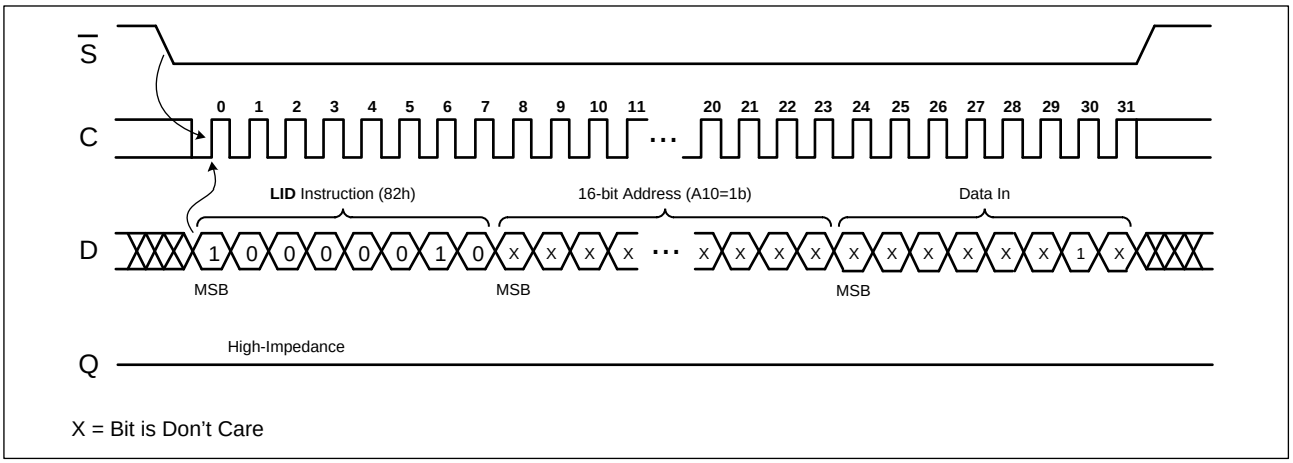
The LID instruction is issued by driving Chip Select ($\overline{S}$) low first, sending the instruction byte (82h), the address bytes and a data byte on Serial Data Input (D), and driving Chip Select ($\overline{S}$) high. Address bit A10 must be '1' and all other address bits are Don't Care. The data byte sent must be equal to the binary value xxxx_xx1x (where x = bit is Don't Care).

Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the LID instruction is not executed (see **Figure 4–12**). Driving Chip Select ($\overline{S}$) high at a byte boundary of the input data triggers the self-timed write cycle, which continues for a period of t_{WC}.

The LID instruction is not executed, under the following conditions:

- If the WEL bit has not been set to '1';
- If a Write cycle is already in progress;
- If the device has not been deselected, by driving high Chip Select ($\overline{S}$), at a byte boundary;
- If the Block Protect bits (BP1, BP0) = (1, 1).

Figure 4–12 Lock Identification Page



4.11 Read Unique ID (RDUID)

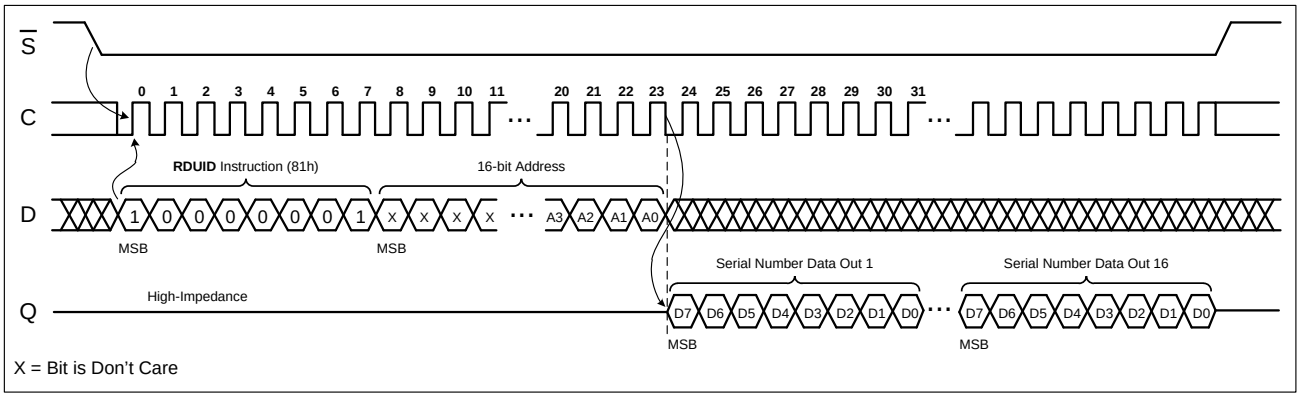
The TD25C128-H offers a separate memory block containing a factory programmed 128-bit Unique ID (UID), or Serial Number. Reading this block is achieved with the Read Unique ID (RDUID) instruction. Chip Select ($\overline{S}$) signal is first driven low; the bits of the instruction byte (81h) and the address bytes are then shifted in on Serial Data Input (D). The upper address bits are Don't Care, and the lower address bits A3:A0 define the byte locations inside the Unique ID block. Then the data byte at this address is shifted out on Serial Data Output (Q). If Chip Select ($\overline{S}$) continues to be driven low, the internal address counter is automatically incremented, and the byte of data at the new address is shifted out (see **Figure 4–13**).

In order to guarantee a unique number, the entire 128-bit value must be read from the starting address of the Serial Number block with the address bits A3:A0 to be '0000'. Reading from a location other than the first address of the block will not result in a unique Serial Number. Writing or altering the 128-bit Unique ID is not allowed. When the end of the 128-bit UID block is reached, the address counter will rollover to the beginning of this block, allowing the read cycle to be continued.

The read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of Chip Select ($\overline{S}$) can occur at any time during the cycle.

The RDUID instruction is not accepted, and is not executed, if a write cycle is currently in progress.

Figure 4–13 Read Unique ID



5 Electrical Specifications

5.1 Absolute Maximum Ratings

Table 5–1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
	Ambient temperature with power applied	-55 to +130	°C
T_{STG}	Storage temperature	-65 to +150	°C
V_{CC}	Supply voltage	-0.5 to +6.0	V
V_{OUT}	Output voltage	-0.5 to V_{CC}+0.5	V
V_{IN}	Input voltage	-0.5 to +6.0	V
I_{OUT}	DC output current	5	mA
V_{ESD}	Electrostatic discharge voltage (human body mode)	6000	V

Note: Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. Functional operation of the device at these ratings or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 DC Characteristics

Operating conditions: T_A = -40°C to +105°C, V_{CC} = 1.7V to 5.5V (unless otherwise noted).

Table 5–2 DC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{CC}	Supply Voltage		1.7	5.5	V
I_{CC1}	Supply Current (Read)	V_{CC}= 1.7V at 5MHz, Q = open	-	1.0	mA
		V_{CC}= 2.5V at 10MHz, Q = open	-	5.0	mA
		V_{CC}= 5.5V at 20MHz, Q = open	-	10	mA
I_{CC2}	Supply Current (Write)	During T_{WC}, $\overline{S}$ = V_{CC}, V_{CC}= 1.7V	-	1.0	mA
		During T_{WC}, $\overline{S}$ = V_{CC}, V_{CC}= 5.5V	-	2.0	mA
I_{SB}	Standby Current	$\overline{S}$ = V_{CC}, V_{CC} = 1.7V	-	20	μA
		$\overline{S}$ = V_{CC}, V_{CC} = 5.5V	-	20	μA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND	-	3.0	μA
I_{LO}	Output Leakage Current	$\overline{S}$ = V_{CC}, V_{OUT} = V_{CC} or GND	-	3.0	μA
V_{IL}	Input Low Voltage	1.7V ≤ V_{CC} < 2.5V	-0.45	0.25*V_{CC}	V
		2.5V ≤ V_{CC} < 5.5V	-0.45	0.3*V_{CC}	V
V_{IH}	Input High Voltage	1.7V ≤ V_{CC} < 2.5V	0.75*V_{CC}	V_{CC}+1	V
		2.5V ≤ V_{CC} < 5.5V	0.7*V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	V_{CC} = 1.7V, I_{OL} = 0.15mA	-	0.2	V
		V_{CC} = 2.5V, I_{OL} = 1.5mA or V_{CC} = 5V, I_{OL} = 2mA	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = 1.7V, I_{OH} = -0.1mA	V_{CC}-0.2	-	V
		V_{CC} = 2.5V, I_{OH} = -0.4mA or V_{CC} = 5V, I_{OH} = -2mA	V_{CC}-0.8	-	V

5.3 AC Characteristics

Operating conditions: T_A = -40°C to +105°C, V_{CC} = 1.7V to 5.5V, C_L = 50pF (unless otherwise noted).

Measurement conditions: Input rise and fall time ≤ 50ns

Input pulse voltages: 0.2*V_{CC} to 0.8*V_{CC}

Input and output timing reference voltages: 0.3*V_{CC} to 0.7*V_{CC}

Table 5–3 AC Characteristics

Symbol	Parameter	V_{CC} ≥ 1.7V		V_{CC} ≥ 1.8V		V_{CC} ≥ 2.5V		V_{CC} ≥ 4.5V		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency	-	2	-	5	-	10	-	20	MHz
t_{WH}	Clock High Time	200	-	80	-	40	-	20	-	ns
t_{WL}	Clock Low Time	200	-	80	-	40	-	20	-	ns
t_{RI}[1]	Input Rise Time	-	200	-	80	-	40	-	15	ns
t_{FI}[1]	Input Fall Time	-	200	-	80	-	40	-	15	ns
t_{CS}	$\overline{S}$ High Time	200	-	60	-	40	-	25	-	ns
t_{CSLS}	$\overline{S}$ Active Setup Time	150	-	60	-	30	-	20	-	ns
t_{CSLH}	$\overline{S}$ Active Hold Time	150	-	60	-	30	-	20	-	ns
t_{CSHS}	$\overline{S}$ Not Active Setup Time	150	-	60	-	30	-	20	-	ns
t_{CSHH}	$\overline{S}$ Not Active Hold Time	150	-	60	-	30	-	20	-	ns
t_{SU}	Data In Setup Time	50	-	20	-	10	-	5	-	ns
t_{HD}	Data In Hold Time	50	-	20	-	10	-	5	-	ns
t_V	Clock Low to Output Valid	-	200	-	80	-	40	-	20	ns
t_{HO}	Output Hold Time	0	-	0	-	0	-	0	-	ns
t_{DIS}	Output Disable Time	-	250	-	100	-	50	-	25	ns
t_{RO}[1]	Output Rise Time	-	200	-	80	-	40	-	15	ns
t_{FO}[1]	Output Fall Time	-	200	-	80	-	40	-	15	ns
t_{SUHD}	$\overline{HOLD}$ Setup Time	50	-	20	-	10	-	5	-	ns
t_{HDHD}	$\overline{HOLD}$ Hold Time	50	-	20	-	10	-	5	-	ns
t_{LZ}	$\overline{HOLD}$ to Output Low-Z	0	250	0	100	0	50	0	25	ns
t_{HZ}	$\overline{HOLD}$ to Output High-Z	-	250	-	100	-	50	-	25	ns
t_{WR}	Write Cycle Time	-	3	-	3	-	3	-	3	ms

Note: [1] This parameter is ensured by characterization only.

Figure 5–1 Serial Input/Output Timing

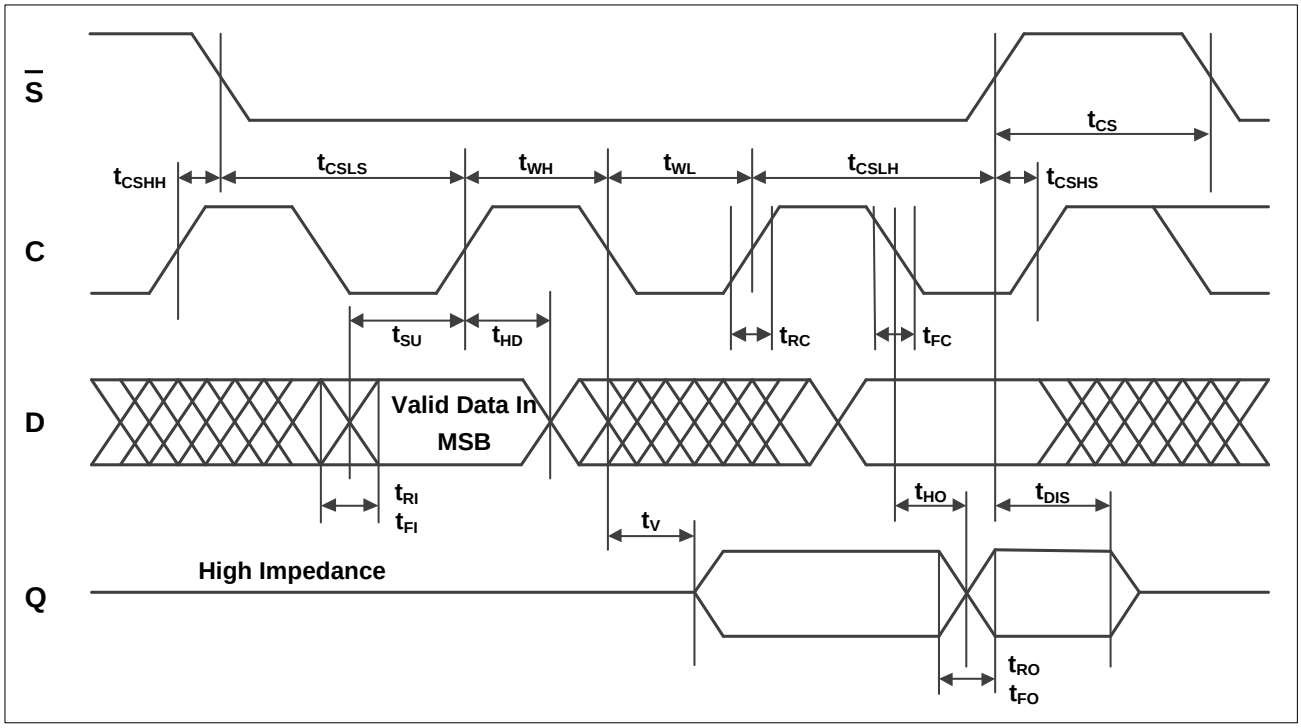
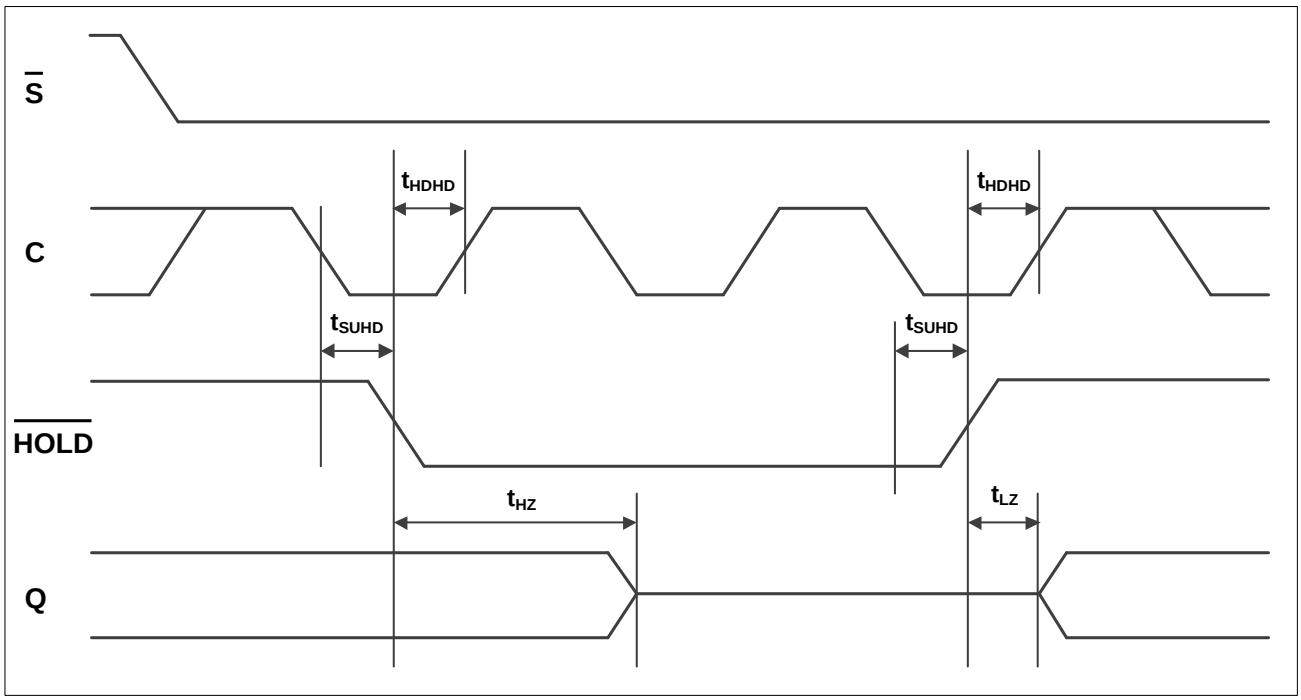


Figure 5–2 Hold Condition Timing



5.4 Pin Capacitance

Operating range for pin capacitance: T_A = +25°C, f_C = 5MHz, V_{CC} = 1.7V to 5.5V.

Table 5–4 Pin Capacitance

Symbol	Parameter[1]	Max	Unit	Test Condition
C_{OUT}	Output Capacitance (Q)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (D)	8	pF	V_{IN} = 0V
C_{IN}	Input Capacitance (other Pins)	6	pF	V_{IN} = 0V

Note: [1] These parameters are ensured by characterization only.

5.5 Reliability Characteristics

Table 5–5 Reliability Characteristics

Symbol	Parameter	Min	Unit	Test Condition
N_W	Write Cycle Endurance	$6x10^6$	cycle	T_A = +25°C, Page Mode
D_R	Data Retention	300	year	T_A = +25°C

6 Power-up and Delivery State

6.1 Power-up State

After power-up, the TD25C128-H is in the following state:

- Standby mode.
- Deselected (a falling edge on Chip Select ($\overline{S}$) is required before any instructions can be started).
- Not in Hold condition.
- The Write Enable Latch (WEL) bit is reset to '0'.
- The Write In Progress (WIP) bit is reset to '0'.
- The SRWD, BP1 and BP0 bits in the Status Register are unchanged from the previous power-down state (they are non-volatile bits).

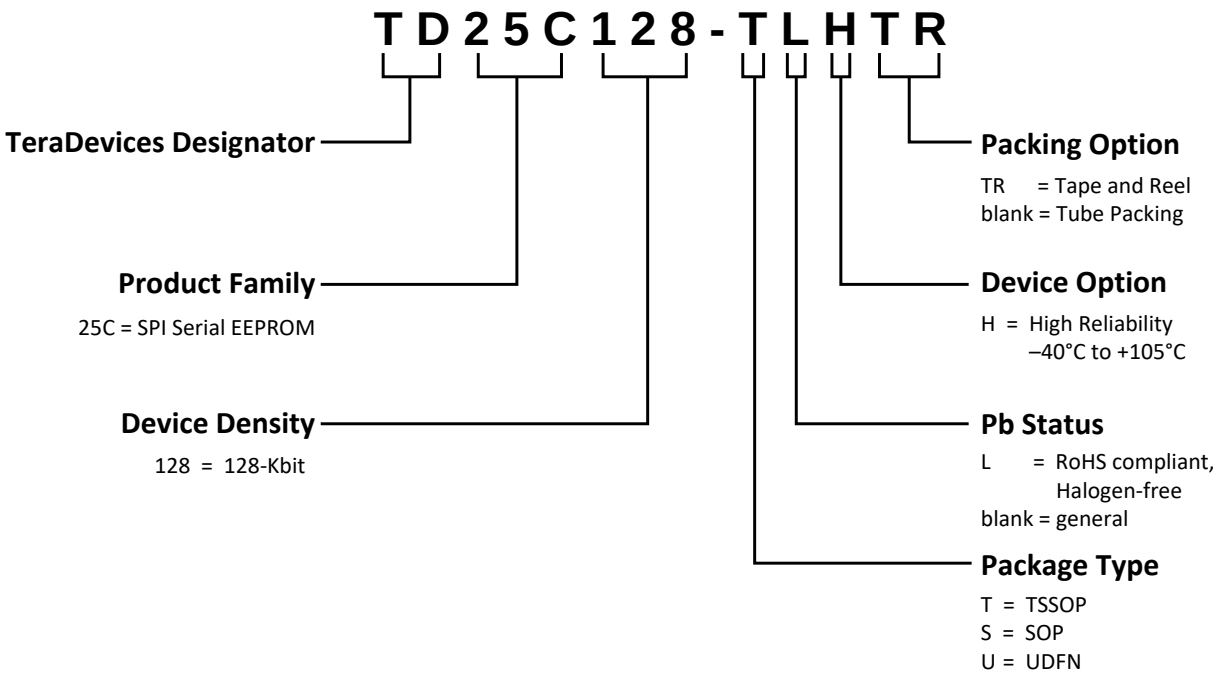
6.2 Initial Delivery State

The TD25C128-H serial EEPROM is delivered as follows:

- All bits in the memory array are set to '1' (each byte contains FFh).
- All bits in the Identification Page are set to '1' (each byte contains FFh).
- The SRWD, BP1 and BP0 bits in the Status Register are initialized to '0'.

7 Ordering Information

Table 7–1 Ordering information scheme

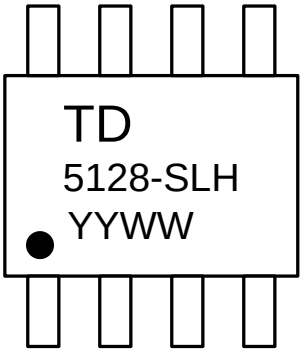


Package types not listed below may be available for order. Please contact TeraDevices for availability details.

Part Number	Package	Delivery Information	Temperature Range
TD25C128-SLHTR	4.9 x 3.9mm SOP	Tape and Reel, 4000 units per Reel	-40°C to +105°C
TD25C128-TLHTR	3.0 x 4.4mm TSSOP	Tape and Reel, 5000 units per Reel	-40°C to +105°C
TD25C128-ULHTR	2.0 x 3.0mm UDFN	Tape and Reel, 3000 units per Reel	-40°C to +105°C

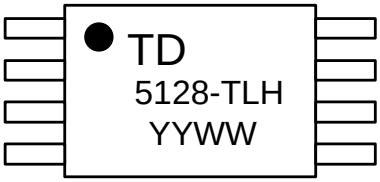
8 Top Markings

8.1 SOP Package Marking



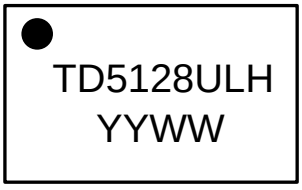
TD: TeraDevices Logo
5128-SLH: TD25C128-SLH
YYWW: Date Code, YY = year, WW = week
Example: 2040 = year 2020 and week 40

8.2 TSSOP Package Marking



TD: TeraDevices Logo
5128-TLH: TD25C128-TLH
YYWW: Date Code, YY = year, WW = week
Example: 2040 = year 2020 and week 40

8.3 UDFN Package Marking

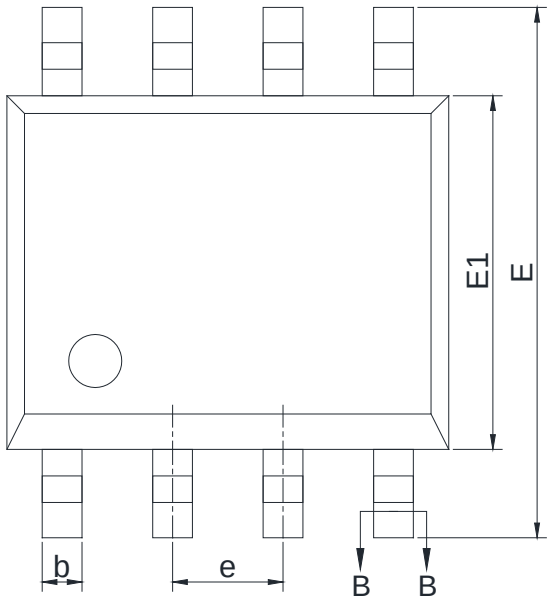


TD: TeraDevices Logo
5128-ULH: TD25C128-ULH
YYWW: Date Code, YY = year, WW = week
Example: 2040 = year 2020 and week 40

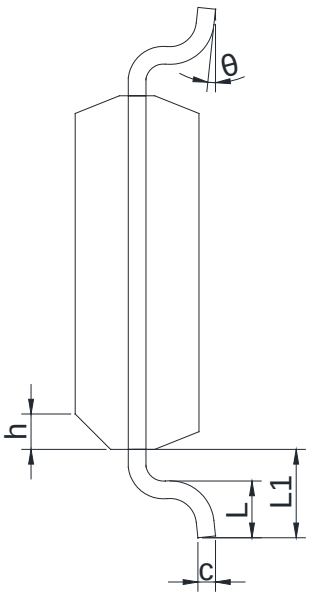
9 Package Information

9.1 SOP Package Information

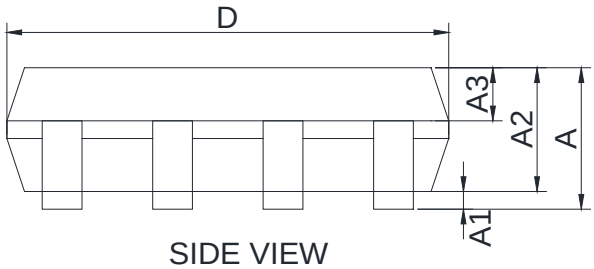
Figure 9–1 8-Lead 4.9 x 3.9mm SOP Package Outline



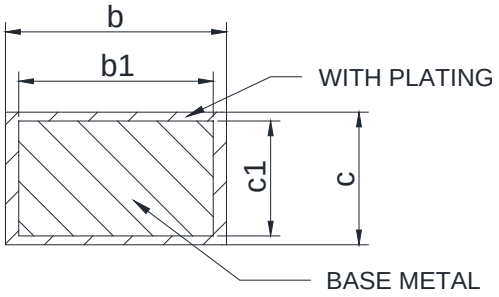
TOP VIEW



END VIEW



SIDE VIEW



SECTION B-B

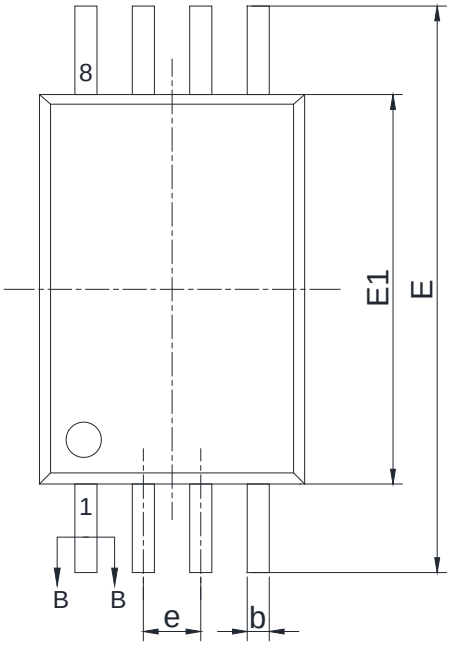
Note:

1. Controlling dimension is mm.
2. Drawing is not to scale.

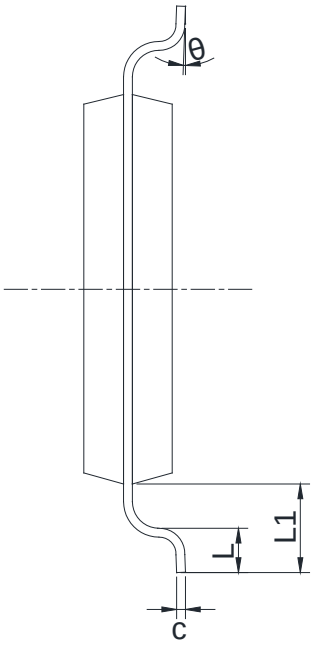
SYMBOL	DIMENSIONS IN MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
E	5.80	6.00	6.20
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

9.2 TSSOP Package Information

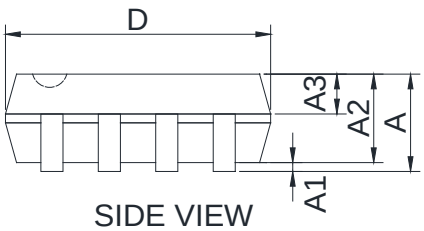
Figure 9–2 8-Lead 3.0 x 4.4mm TSSOP Package Outline



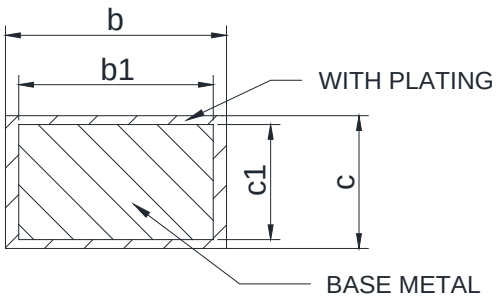
TOP VIEW



END VIEW



SIDE VIEW



SECTION B-B

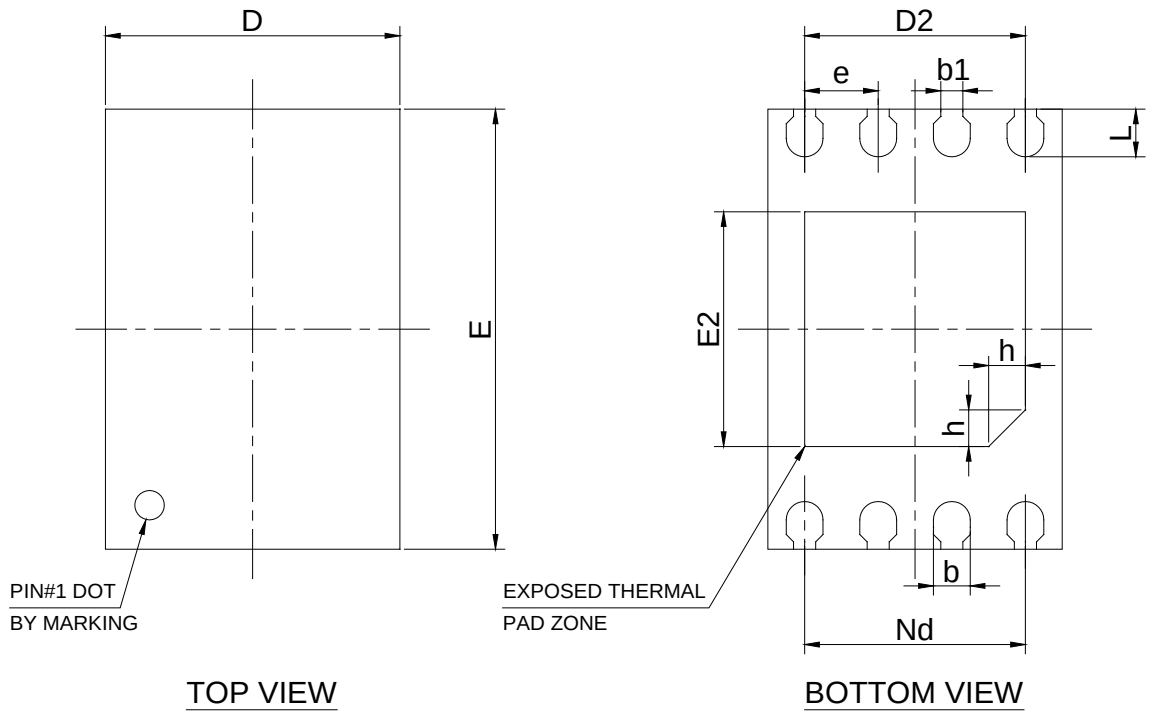
Note:

1. Controlling dimension is mm.
2. Drawing is not to scale.

SYMBOL	DIMENSIONS IN MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	2.90	3.00	3.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	8°

9.3 UDFN Package Information

Figure 9–3 8-Pad 2.0 x 3.0mm UDFN Package Outline



SYMBOL	DIMENSIONS IN MILLIMETER		
	MIN	NOM	MAX
A	0.45	0.50	0.55
	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.18	0.25	0.30
b1		0.16REF	
c	0.10	0.15	0.20
D	1.90	2.00	2.10
D2	1.40	1.50	1.60
e		0.50BSC	
Nd		1.50BSC	
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
L	0.30	0.40	0.50
h	0.20	0.25	0.30

Note:

1. Controlling dimension is mm.
2. Drawing is not to scale.
3. Default thickness marked by symbol A is 0.55mm (NOM), 0.50mm (NOM) is an alternative if needed.

10 Revision History

Revision	Date	Comments
Rev.1.0	Dec. 2020	Initial version release
Rev.1.1	Oct. 2021	Updated: — *Features* and *Description* — t_{INIT} value in *Table 3–1* — I_{CC1}, I_{CC2}, I_{SB} value in *Table 5–2* — AC timing symbols in *Figure 5–1* Added: — AC Characteristics when $V_{CC} \geq 1.7V$ in *Table 5–3* — t_{CSLS}, t_{CSLH}, t_{CSHS}, t_{CSHH} value in *Table 5–3*