TD24C64-C1

64-Kbit I^2C Serial EEPROM 4-ball WLCSP

DATASHEET Rev.1.2

Features

- Supply Voltage Range: 1.7V to 5.5V
- 2-wire Serial Interface I^2C Compatible
  - 400 kHz and High Speed 1MHz Transfer Rate Compatibility
- Byte and Page (up to 32 bytes) Write Mode, Partial Page Write Allowed
- Software Write Protection on the Whole Memory Array
- Software Programmable Device Address Configuration
- Additional 32-byte Write Lockable Page and 128-bit Unique ID
- Self-timed Write Cycle (3ms Maximum)
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- High Reliability
  - Endurance: 2,000,000 Write Cycles
  - Data Retention: 200 Years
  - ESD Protection (Human Body Model): 6000V
- Low Operating Current
  - Write Current: 0.5mA (Maximum)
  - Read Current: 0.5mA (Maximum)
  - Standby Current: 1μA (Maximum)
- Operating Temperature Range: -40°C to +105°C
- Green Packaging Option (RoHS Compliant, Pb/Halogen-free)
  - 4-ball WLCSP with Ball Pitch: 400μm X 400μm

Description

The TD24C64-C1 is a 64-Kbit I^2C-compatible serial EEPROM organized as 256 pages of 32 bytes each, totaling 8192*8 bits. The device is designed to operate in a supply voltage range of 1.7V to 5.5V, with a maximum of 1MHz transfer rate, over an operating temperature range of -40°C to +105°C.

The TD24C64-C1 offers an additional 8-bit Chip Enable register for the Device Address Configuration (DAC) and Software Write Protection (SWP) feature. The device address is configurable through software, allowing up to eight devices on the bus at the same time. Write Protection of the whole memory array is software programmable by setting the SWP bit value.

The TD24C64-C1 offers an additional 32-byte Identification Page for users to store sensitive application parameters. The Identification Page can be locked in Read-only mode permanently after the data is written into this page. The device also offers a separate memory block (in Read-only mode) containing a factory programmed 128-bit Unique ID.

The TD24C64-C1 is delivered in a 4-ball WLCSP package.

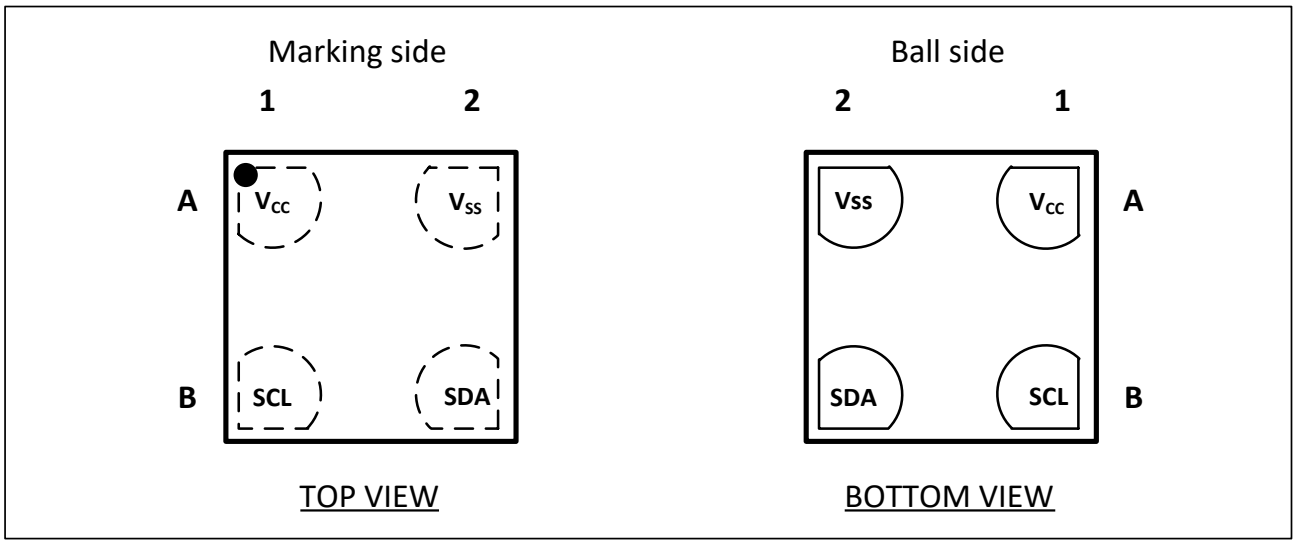
Table of Contents

1 Pin Descriptions and Pin Configuration

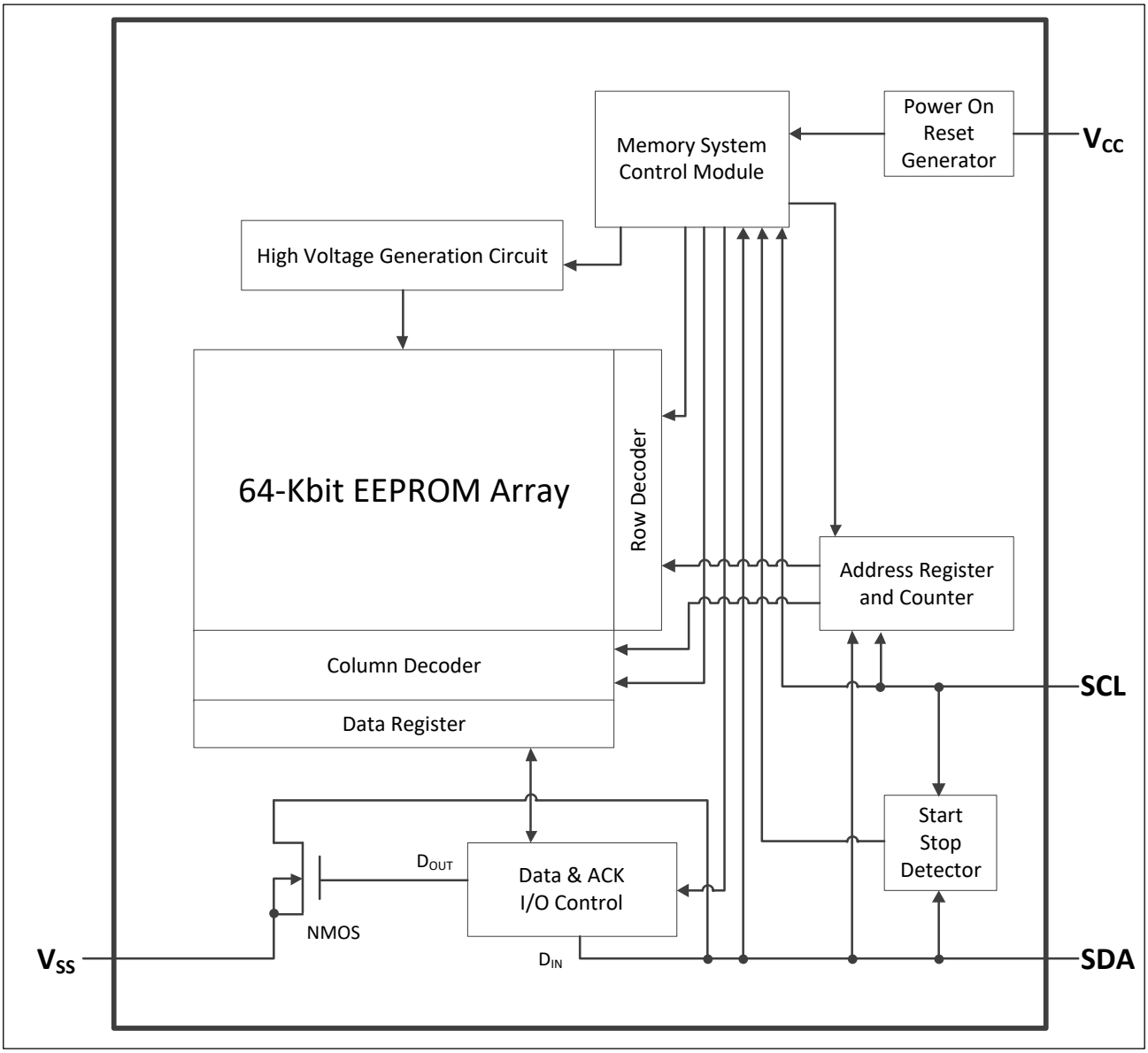
Table 1–1 Pin Descriptions

Symbol	Type	Name and Function
SDA	Input/Output	**Serial Data:** The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device.
SCL	Input	**Serial Clock:** The SCL pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is always clocked out on the falling edge of SCL.
V_{CC}	Power	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.
V_{SS}	Ground	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.

Figure 1–1 Pin Configuration of 4-ball WLCSP (Ball Pitch 400μm X 400μm)



2 Functional Block Diagram



3 Features for WLCSP Package Device

3.1 Chip Enable Register

As the TD24C64-C1 is delivered in 4-ball WLCSP without Device Address inputs and Write Protection pin, the device provides a non-volatile 8-bit register, called Chip Enable register, allowing users to define a configurable device address by Device Address Configuration (DAC) feature and write-protect the whole memory array by Software Write Protection (SWP) feature. This register can be written and read with the device type identifier of '1010' at a specific word address. The description of the Chip Enable register is given in **Table 3–1**.

Table 3–1 Chip Enable Register (Address 1xxx_xxxx_xxxx_xxx0b)

Register Data Byte							
bit 7	bit 6	bit 5	bit 4	bit 3[2]	bit 2[2]	bit 1[2]	bit 0
X[1]	X	X	X	Device Address Configuration E2 (bit 3), E1(bit 2), E0 (bit1)			Software Write Protect Activation 0: the whole memory can be written 1: the whole memory is write-protected

Notes: [1] X = Bit is Don't Care.

[2] Bits 3:1 Device Address Configuration:

(b3,b2,b1) = (0,0,0): the device address is 000 (factory default state)

(b3,b2,b1) = (0,0,1): the device address is 001

(b3,b2,b1) = (0,1,0): the device address is 010

(b3,b2,b1) = (0,1,1): the device address is 011

(b3,b2,b1) = (1,0,0): the device address is 100

(b3,b2,b1) = (1,0,1): the device address is 101

(b3,b2,b1) = (1,1,0): the device address is 110

(b3,b2,b1) = (1,1,1): the device address is 111

3.2 Device Address Configuration

Bit 3, bit 2 and bit 1 define the device address bits E2, E1 and E0 in the Device Address Byte, respectively. These four bits can be written and reconfigured with a Write command (see **Section 5.1.5**). Factory default state of the bit 3, bit 2 and bit 1 is 000b.

Note that the software device address bits (E2, E1 and E0) must match the corresponding address data (bit 3, bit 2 and bit 1). After the values of bit 3, bit 2 and bit 1 are reconfigured, the Master should send new device address bits for the subsequent instructions, otherwise the device responds with a NACK.

3.3 Software Write Protection

In order to prevent unwanted Write operations, the TD24C64-C1 offers a SWP bit (bit 0 in Chip Enable register), which makes it possible to protect the content in the whole 64-Kbit memory array. Updating the SWP bit to a new value is a reversible action with a Write command (see **Section 5.1.5**). The SWP bit can be updated from 0 to 1 and from 1 to 0. Write operations are disabled (Read-only memory) when the SWP bit is set to Logic 1, while Write operations are enabled when the SWP bit is set to Logic 0. Upon a certain instruction send by the Master, the device will automatically load the last configuration of the SWP bit.

4 Device Communication

The TD24C64-C1 operates as a slave device and utilizes a 2-wire serial interface to communicate with the Master. The Master initiates and controls all Read and Write operations to the slave devices on the serial bus, and both the Master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: the Serial Clock (SCL) and the Serial Data (SDA). Data is always latched into the TD24C64-C1 on the rising edge of SCL and is always output from the device on the falling edge of SCL. Both the SCL pin and SDA pin incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

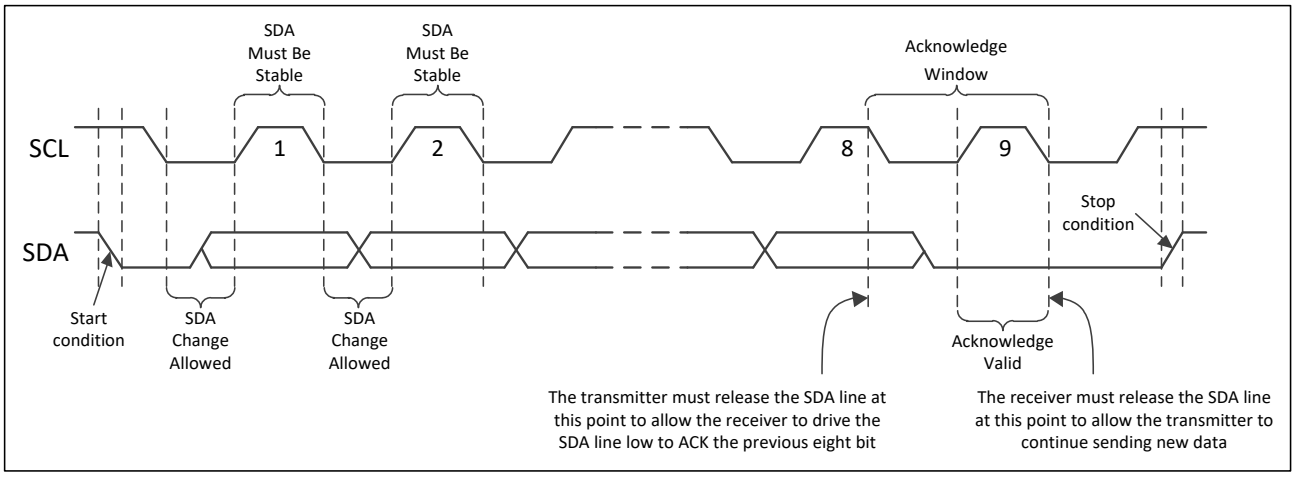
All command and data information is transferred with the Most Significant Bit (MSB) first. During the bus communication, one data bit is transmitted every clock cycle, and after eight bits of data has been transferred, the receiving device must respond with an acknowledge or a no-acknowledge response bit during a ninth clock cycle generated by the Master. Therefore, nine clock cycles are required for every one byte of data transferred. There is no unused clock cycle during any Read or Write operation, so there must not be any interruptions or breaks during the data stream.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the Master.

4.1 Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is stable in Logic 1 state. The Start condition must precede any command as the Master uses a Start condition to initiate any data transfer sequence (see **Figure 4–1**). The TD24C64-C1 will continuously monitor the SDA and SCL pins for a Start condition, and the device will not respond unless one is given.

Figure 4–1 Start, Stop, and ACK



4.2 Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in Logic 1 state (see **Figure 4–1**). A stop condition terminates communication between the TD24C64-C1 and the Master. A Stop condition at the end of a Write command triggers the EEPROM internal write cycle. Otherwise, the TD24C64-C1 subsequently returns to Standby mode after receiving a Stop condition.

4.3 Acknowledge (ACK)

After each byte of data is received, the TD24C64-C1 should acknowledge to the Master that it has received the data byte successfully. This is accomplished by the Master first releasing the SDA line and providing the ACK/NACK clock cycle (a ninth clock cycle for every byte). During the ACK/NACK clock cycle, the TD24C64-C1 must output Logic 0 as ACK for the entire clock cycle so that the SDA line must be stable in Logic 0 state during the entire high period of the clock cycle (see **Figure 4–1**).

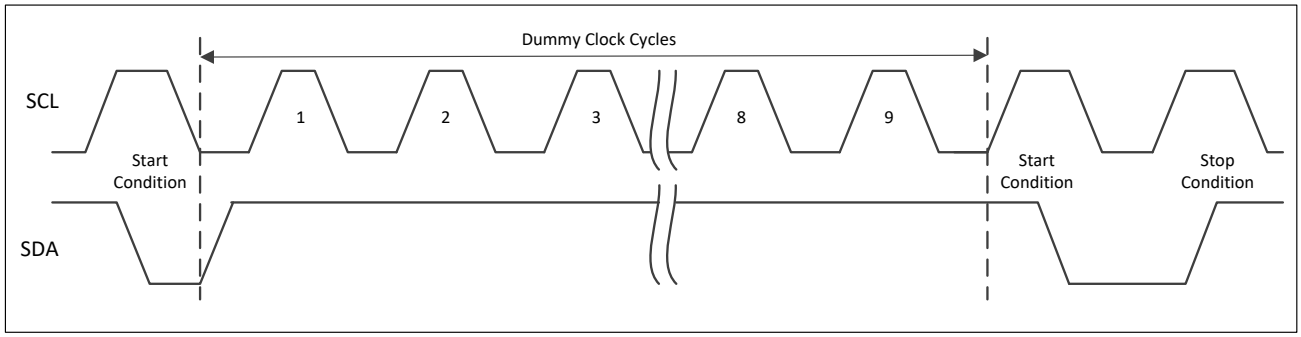
4.4 Standby Mode

The TD24C64-C1 features a low-power Standby mode which is enabled:
(1) Upon power-up;
(2) After the receipt of a Stop condition in Read operation;
(3) The completion of any internal operations.

4.5 Software Reset

After an interruption in protocol, power loss, or system reset, any 2-wire part can be reset by following these steps: (1) Create a Start condition; (2) Clock nine cycles; (3) Create another Start condition followed by a Stop condition (see **Figure 4–2**).

Figure 4–2 2-wire Software Reset



4.6 Device Reset and Initialization

The TD24C64-C1 incorporates a Power-On Reset (POR) circuit to prevent inadvertent operations during power-up. On a cold power-up, the device does not respond to any instructions until the supply voltage reaches the internal power-on reset threshold voltage (V_{POR}). The supply voltage must rise continuously between V_{POR} and V_{CC}(Min) without any ring back to ensure a proper power-up. Once the supply voltage passes V_{POR}, the device is reset and enters Standby mode. However, no protocol should be issued to the device until a valid and stable supply voltage is applied for the time specified by the t_{INIT} parameter. The supply voltage must remain stable and valid until the end of the protocol transmission, and for a Write instruction, until the end of the internal write cycle (see **Figure 4–3**).

This POR behavior is bi-directional. It protects the TD24C64-C1 against brown-out failure caused by a temporary loss of power. In a similar way, as soon as the supply voltage drops below the internal brown-out reset threshold voltage (V_{BOR}), the device is reset and stops responding to any instructions. The V_{BOR} level is set below the V_{POR} level.

Parameters related to power-up and power-down conditions are listed in **Table 4–1**.

Figure 4–3 Power-up and Power-down Timing

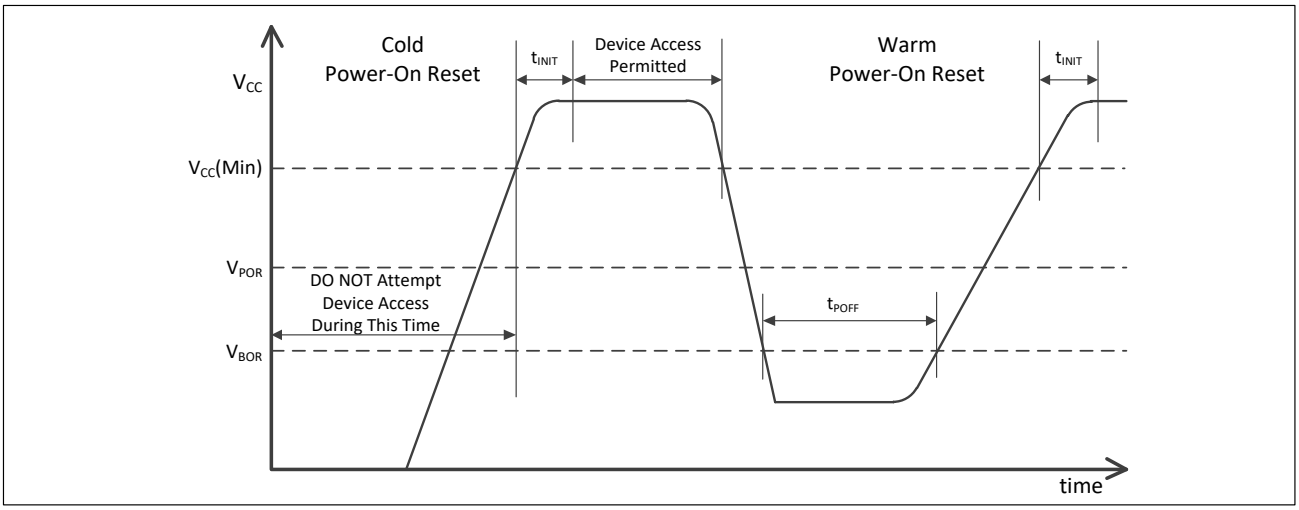


Table 4–1 Power-up and Power-down Conditions

Symbol	Parameter	Min	Max	Unit
V_{POR}	Power-On Reset Voltage	-	1.5	V
V_{BOR}	Brown-Out Reset Voltage	1.3	-	V
t_{INIT}	Time from V_{CC}(Min) to First Command	100	-	μs
t_{POFF}	Warm Power Cycle Off Time	100	-	μs

4.7 Data Security

The TD24C64-C1 offers a Software Write Protection (SWP) feature that allows users to write protect the whole memory array when the internal non-volatile SWP bit is set to Logic 1 (see **Section 3.3** for details).

4.8 Device Addressing

The TD24C64-C1 requires a 7-bit device address and a Read/Write select bit following a Start condition from the Master to initiate communication with the serial EEPROM. The device address byte is comprised of a 4-bit device type identifier followed by three device address bits (E2, E1, and E0) and a R/$\overline{W}$ select bit and is clocked by the Master on the SDA pin with the most significant bit (bit 7) first.

The TD24C64-C1 will respond to two unique device type identifiers. The device type identifier of ‘1010’ is necessary to select the device 64-Kbit memory for normal Read or Write operation. The device type identifier of ‘1010’ is also used to select the Chip Enable register for Read or Write operation. The device type identifier of ‘1011’ is used to select the Identification Page for Read or Write / Lock operation. The device type identifier of ‘1011’ is also used for Read Unique ID operation (see **Table 4–2**).

The software device address bits (E2, E1 and E0) must match the corresponding device address data stored in the Chip Enable register, allowing up to eight devices on the bus at the same time. The eighth bit of the address byte is the R/$\overline{W}$ operation selection bit. A Read operation is selected if this bit is Logic 1, and a Write operation is selected if this bit is Logic 0. Upon a compare of the device address byte, the TD24C64-C1 outputs an ACK or a NACK during the ninth clock cycle if the compare is true or not true, respectively. The device will return to the low-power Standby mode after a NACK.

Once the TD24C64-C1 has acknowledged the device address byte, the device waits for the Master to send two

word address bytes (first word address byte sent first, followed by the second word address byte) for a certain Read or Write instruction according to **Table 4–3**. The TD24C64-C1 responds to each address byte with an ACK.

Table 4–2 TD24C64-C1 Device Address Byte

Function	Device Type Identifier				Device Address			Read/Write
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
When accessing the 64-Kbit memory array	1	0	1	0	E2	E1	E0	$R/\overline{W}$
When accessing the Chip Enable register	1	0	1	0	E2	E1	E0	$R/\overline{W}$
When accessing the Identification Page	1	0	1	1	E2	E1	E0	$R/\overline{W}$
When accessing the Lock Identification Page bit	1	0	1	1	E2	E1	E0	0
When accessing the Unique ID	1	0	1	1	E2	E1	E0	1

Table 4–3 TD24C64-C1 Word Address Bits

Function	First Word Address Byte								Second Word Address Byte							
	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Random Read	0	X[1]	X	A12[2]	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Byte/Page Write	0	X	X	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Write Chip Enable Register	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Read Chip Enable Register	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Read Identification Page	X	X	X	X	X	0	0	X	X	X	X	A4	A3	A2	A1	A0
Write Identification Page	X	X	X	X	X	0	0	X	X	X	X	A4	A3	A2	A1	A0
Lock Identification Page	X	X	X	X	X	1	0	X	X	X	X	X	X	X	X	X
Read Lock Status	X	X	X	X	X	0	0	X	X	X	X	X	X	X	X	X
Read Unique ID	X	X	X	X	X	0	1	X	X	X	X	X	A3	A2	A1	A0

Notes: [1] X = Bit is Don't Care.

[2] A = Significant address bit.

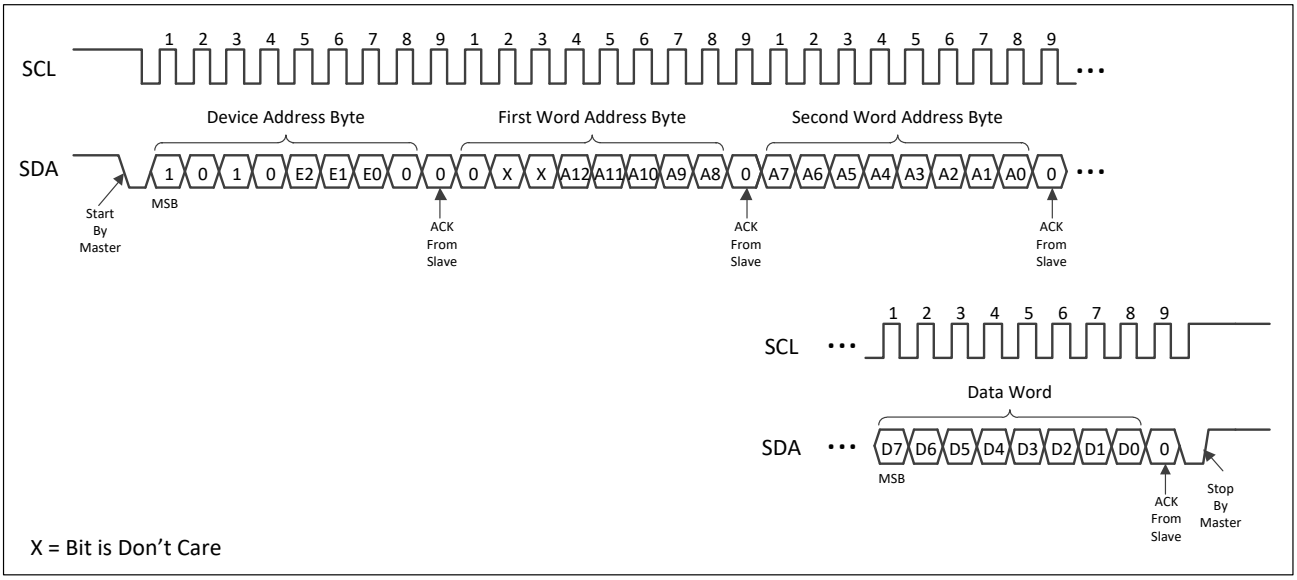
5 Read and Write Operations

5.1 Write Operations

5.1.1 Byte Write

For a Byte Write operation, the Master sends a Start condition followed by the device type identifier of '1010', the device address bits and the R/$\overline{W}$ select bit set to Logic 0. The TD24C64-C1 responds with an ACK during the ninth clock cycle and waits for the Master to send two word address bytes (first word address byte and second word address byte). Then the device responds to each word address byte with an ACK. After receiving ACKs from the device, the Master transmits one data byte. If the addressed location has been Write-protected, the device responds with a NACK, and the addressed location will not be modified. If the addressed location is not Write-protected, the device responds with an ACK. The Master ends the Byte Write sequence with a Stop condition during the 10th clock cycle to initiate the internally self-timed write cycle (see **Figure 5–1**). A Stop condition issued during any other clock cycle during the Write operation will not trigger the internal write cycle. Once the write cycle begins, the preloaded data word will be programmed in the amount of time not to exceed the t_{WR} specification (see **Figure 5–3**). During the time, the Master should wait a fixed time by the t_{WR} specification, or for time sensitive applications, an ACK polling routine can be implemented. All inputs are ignored by the device during the write cycle and the device will not respond until the write cycle is completed. The serial EEPROM will increment its internal address counter each time a byte is written.

Figure 5–1 Byte Write



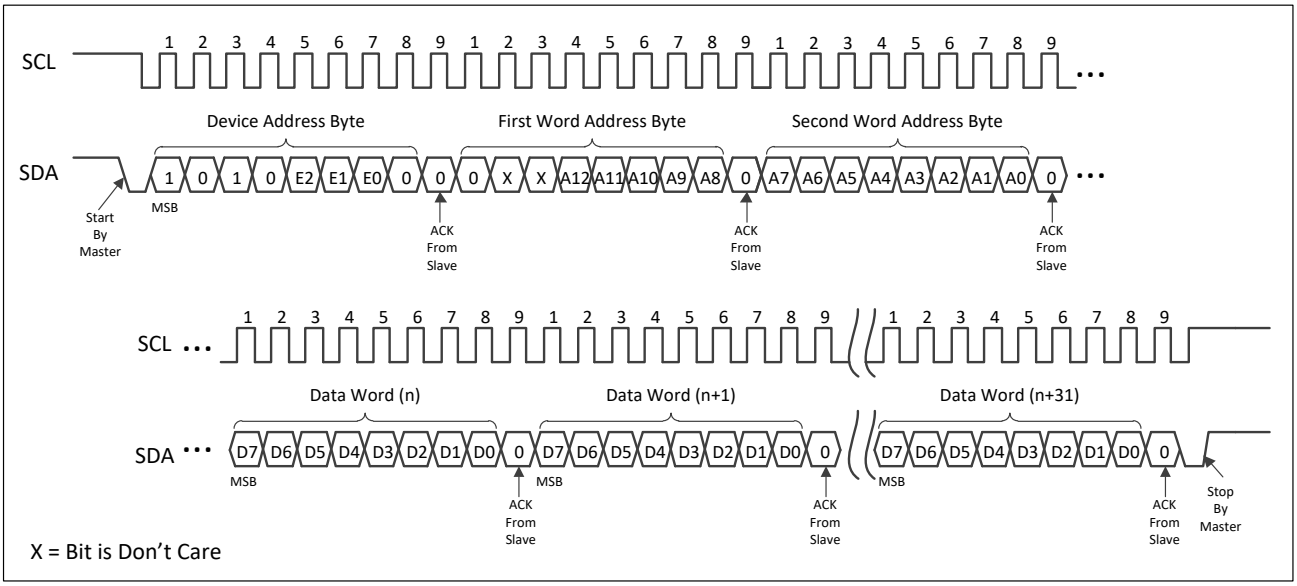
5.1.2 Page Write

The 64-Kbit serial EEPROM is capable of writing up to 32 data bytes at a time by executing the Page Write protocol sequence. A partial or full Page Write operation is initiated the same as a Byte Write operation except that the Master does not send a Stop condition after the first data word is clocked in. Instead, after the device has acknowledged to the first data word, the Master can transmit up to thirty-one more data words. The device responds with an ACK after each data word is received if the addressed locations are not Write-protected. If the addressed locations have been Write-protected, the device responds with a NACK to each data word and the addressed locations will not be modified. After the device acknowledges to the last data word, the Master should end the Page Write sequence with a Stop condition to initiate the internal write cycle (see **Figure 5–2**).

A Stop condition issued at any other clock cycle will not initiate the internally self-timed write cycle and the Write sequence will have to be repeated again. Once the write cycle begins, the data words should be programmed in the amount of time not exceeding the t_{WR} specification (see **Figure 5–3**). During this time, the Master should wait a fixed time by the t_{WR} specification, or for time sensitive applications, an ACK polling routine can be implemented.

The lower five bits of the word address are internally incremented following the receipt of each data word. The higher word address bits are not incremented, retaining the memory page row location. When the internally generated word address reaches the page boundary, the following data word will be placed at the beginning of the same page. If more than thirty-two data words are transmitted to the device, the data word address will roll over and the previous data will be overwritten. The address roll-over during a Write sequence is from the last byte of the current page to the first byte of the same page.

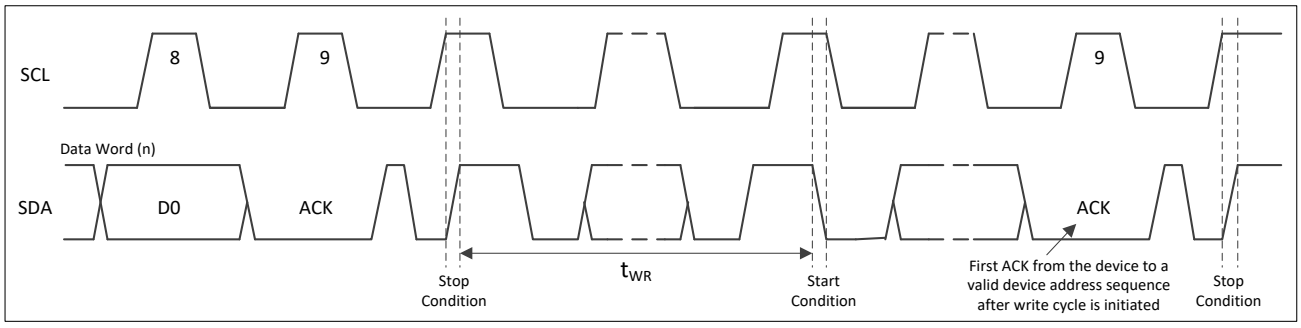
Figure 5–2 Page Write



5.1.3 Write Cycle Timing

The length of the self-timed write cycle, or t_{WR}, is defined as the amount of time from a valid Stop condition that begins the internal write sequence to the Start condition of the first device address byte sent to the TD24C64-C1 that it subsequently responds to with an ACK (see **Figure 5–3**).

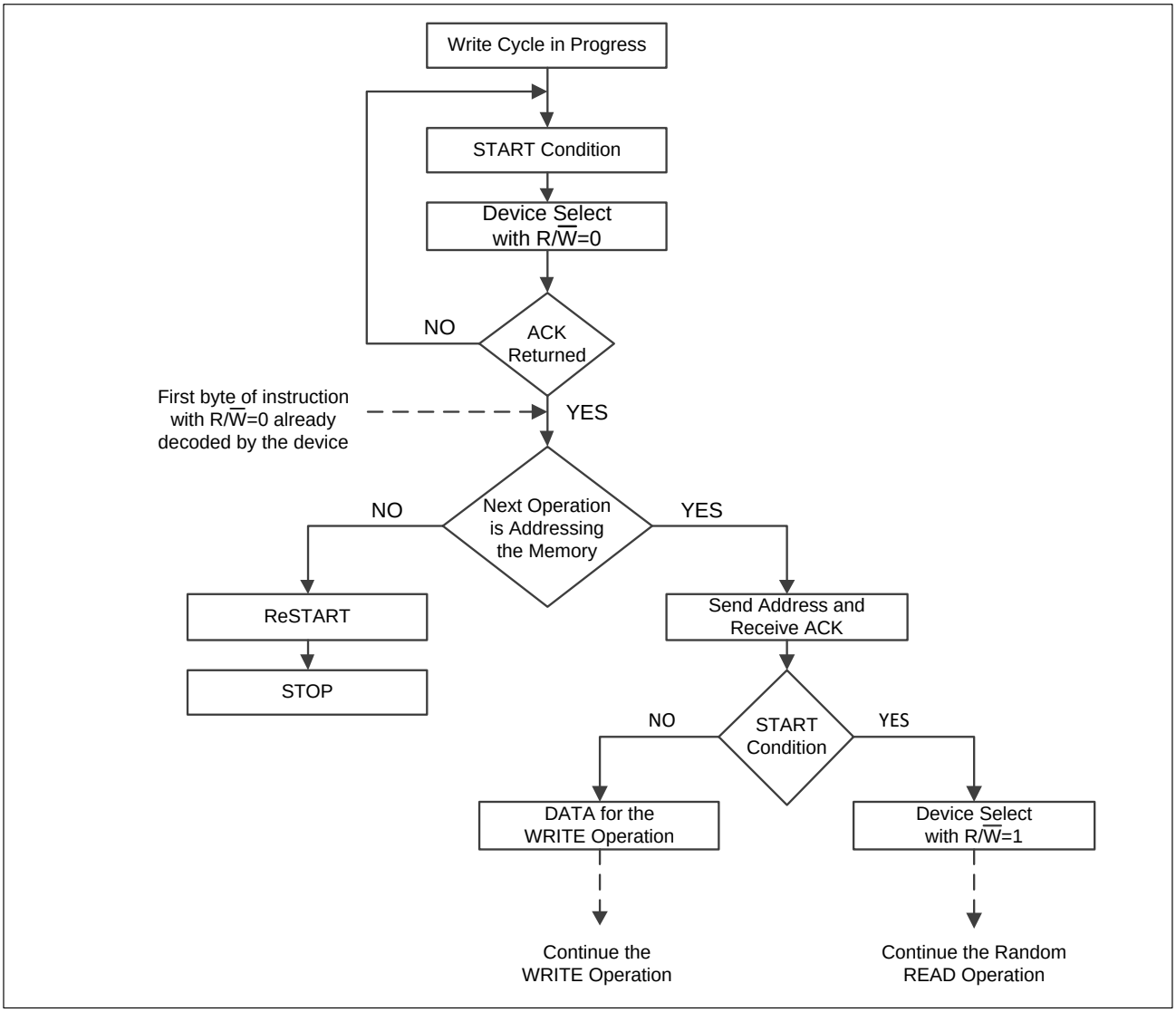
Figure 5–3 Write Cycle Timing



5.1.4 Acknowledge (ACK) Polling

An ACK polling routine can be implemented to optimize time sensitive applications that would not prefer to wait the fixed maximum write cycle time but would prefer to know immediately when the serial EEPROM write cycle has completed to start a subsequent operation. Once the internally self-timed write cycle has started, the device inputs are disabled and ACK polling can be initiated. An ACK polling routine involves sending a valid Start condition followed by the device address byte. While the write cycle is in progress, the device will not respond with an ACK, indicating the device is busy writing data. Once completed, the device returns an ACK and the next device operation can be started (see **Figure 5–4**).

Figure 5–4 Acknowledge Polling Flow Chart



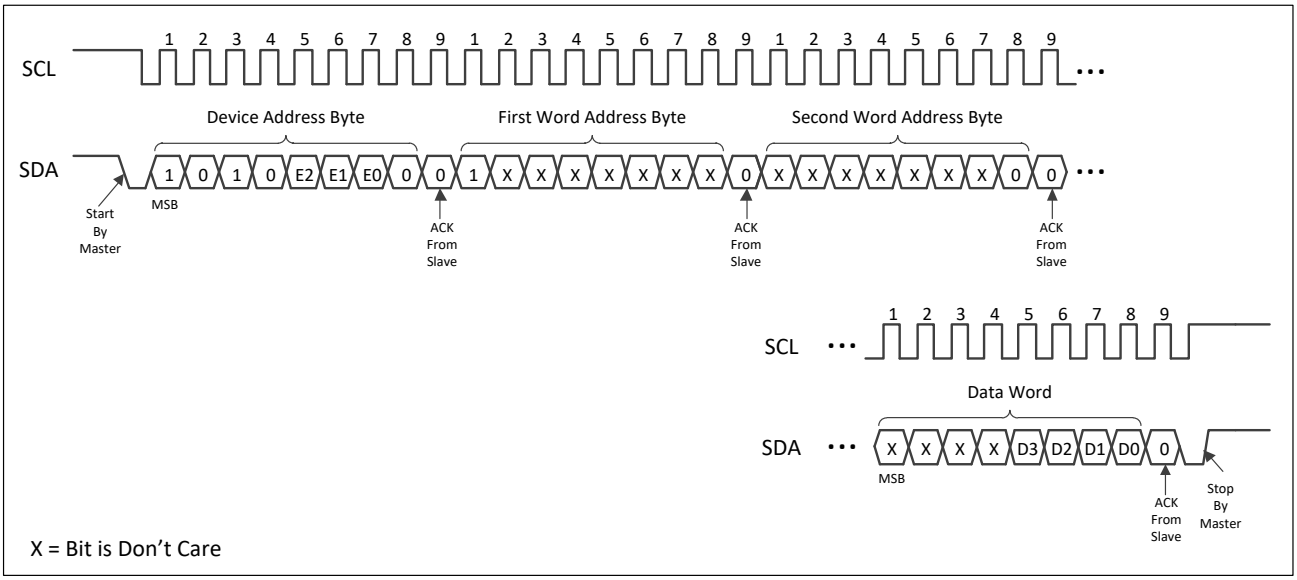
Notes: In case of writing Chip Enable register when E2, E1 and E0 are reconfigured, the device will return ACK only if:
three device address bits of the Device Address Byte is equal to the new E2, E1 and E0 values;
internal write cycle is completed (new E2, E1 and E0 values have been programmed in the Chip Enable register).

5.1.5 Write Operation on Chip Enable Register

The TD24C64-C1 provides a non-volatile 8-bit register for users to achieve Device Address Configuration (DAC) and Software Write Protection (SWP) feature. Writing in the Chip Enable register can be performed with a Byte Write instruction at address 1xxx_xxxx_xxxx_xxx0b (where 'x' is Don't Care), as shown in **Figure 5–5**. The data word byte is defined in **Table 3–1**.

Write Chip Enable register is performed independently of the state of SWP bit. Writing more than one byte will discard the write cycle and the content in the Chip Enable register will not be changed.

Figure 5–5 Write Chip Enable Register



5.1.6 Write Identification Page

The TD24C64-C1 offers a 32-byte Identification Page (ID Page) in addition to the 64-Kbit memory array for storage of specific application data. This Identification Page can be written and permanently locked in Read-only mode after the data is written into this Page. The Identification Page is written by issuing the Write Identification Page instruction (see **Figure 5–6**), which uses the same protocol and format as Page Write, except that:

- The device type identifier is defined as '1011';
- The word address bits A10:A9 must be '00', bits A15:A11 and A8:A5 are Don't Care;
- The word address bits A4:A0 define the byte locations inside the ID Page (see **Table 4–3**).

If the Identification Page has been locked, the data bytes transferred during the Write Identification Page instruction will not be acknowledged.

5.1.7 Lock Identification Page

The Lock Identification Page (Lock ID) instruction permanently locks the Identification Page in Read-only mode. The Lock ID instruction is similar to Byte Write, except the following specific conditions:

- The device type identifier is defined as '1011';
- The word address bits A10:A9 must be '10' and other word address bits are Don't Care;
- The data byte must be equal to the binary value xxxx_xx1x, where 'x' is Don't Care (see **Figure 5–7**).

Once a valid Lock ID instruction has been executed, if another Lock ID instruction is issued, the device will respond with a NACK to the data word byte.

Figure 5–6 Write Identification Page

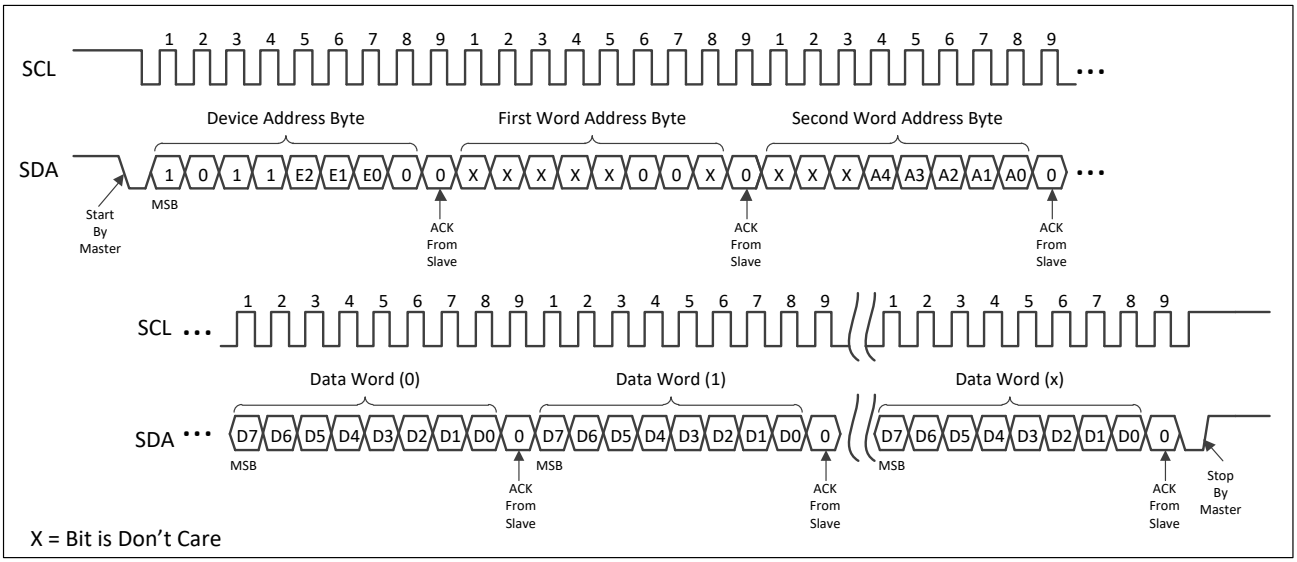
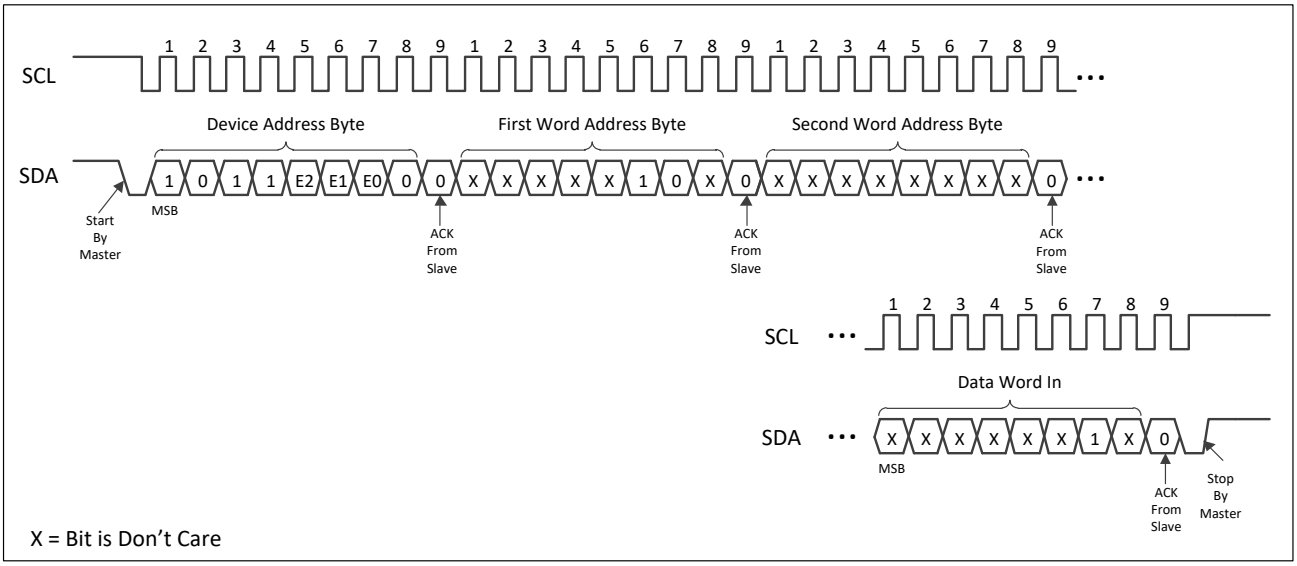


Figure 5–7 Lock Identification Page



5.2 Read Operations

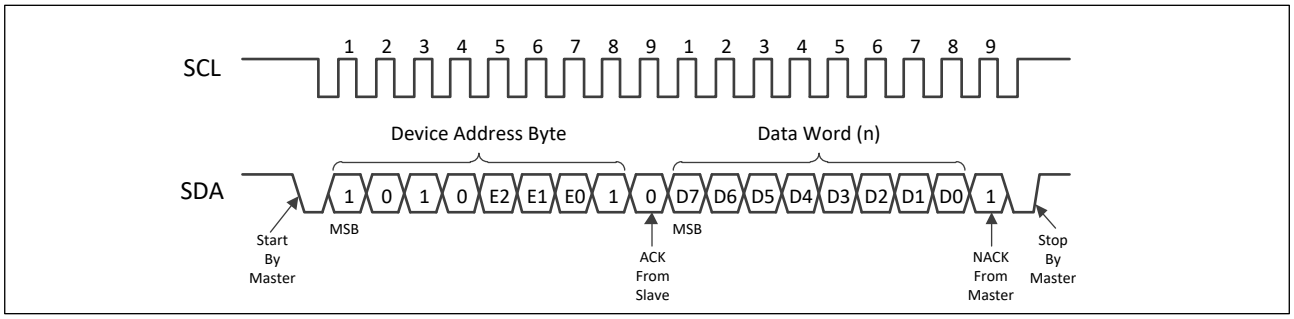
All Read operations are initiated by the Master transmitting a Start condition, a device type identifier of ‘1010’ or ‘1011’, three software device address bits (E2, E1, E0) that match corresponding values in Chip Enable register, and the R/$\overline{W}$ select bit with Logic 1 state. In the following clock cycle, the TD24C64-C1 should respond with an ACK. The subsequent protocol depends on the type of Read operation desired. There are three Read operations for memory array: Current Address Read, Random Address Read, and Sequential Read with the device type identifier of ‘1010’; two Read operations for functional registers: Read Chip Enable register and Read Write Protection Status with the device type identifier of ‘1010’; three Read operations for Identification Page and Unique ID: Read Identification Page, Read the Lock Status, and Read Unique ID with the device type identifier of ‘1011’.

5.2.1 Current Address Read

For a Current Address Read operation, the Master sends a Start condition followed by transmitting the device address byte with the R/$\overline{W}$ bit set to Logic 1 (see **Figure 5–8**). The TD24C64-C1 should respond with an ACK and then serially transmits the data word addressed by the internal address counter. This address maintained by the internal address counter is the last address accessed during the last Read or Write operation. The counter is then incremented by one and the address will stay valid between operations as long as power to the device is supplied. The address roll-over during a Read operation is from the last byte of the last page to the first byte of the first page. To end the command, the Master responds with a NACK followed by a Stop condition.

Note that the address counter value is defined by instructions accessing the memory or the Chip Enable register or the ID Page or the Unique ID. For example, when accessing the ID Page, the counter value is loaded with the byte location in the ID Page. Therefore the next Current Address Read in the memory uses this new address counter value. When accessing the memory, it is recommended to always use the Random Read instruction (see **Section 5.2.2**) instead of the Current Address Read instruction.

Figure 5–8 Current Address Read

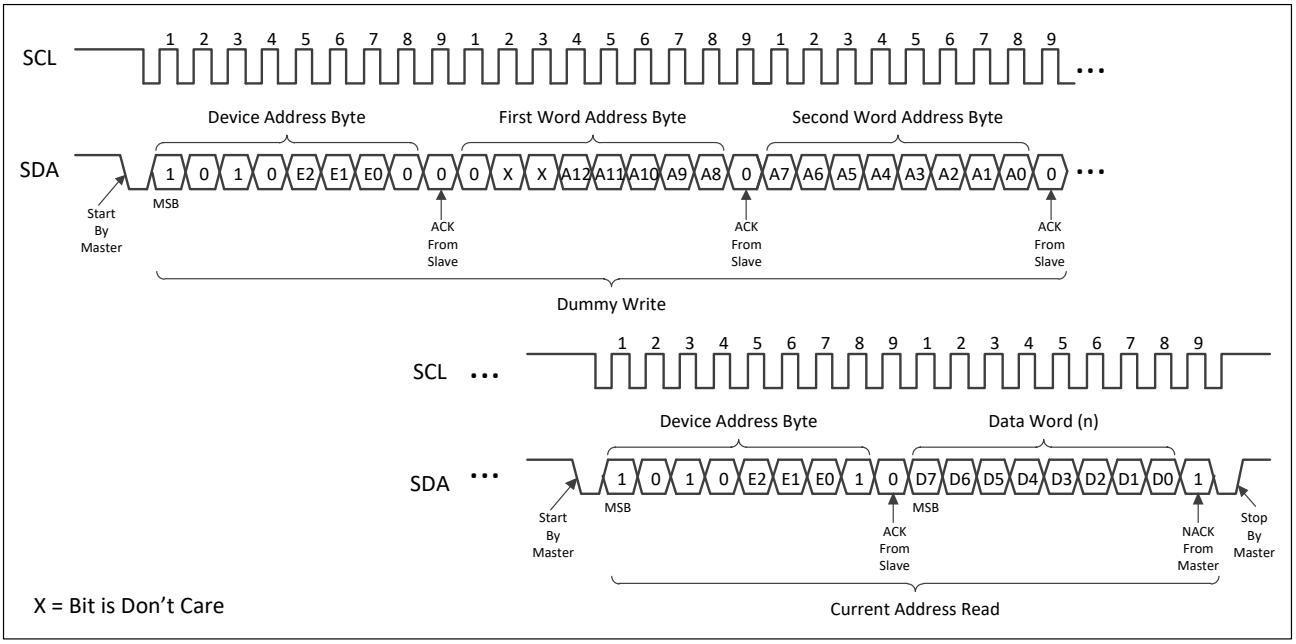


5.2.2 Random Read

A Random Read operation allows the Master to access any memory location in a random manner and requires a dummy write sequence to preload the starting data word address. To perform a Random Read, the device address byte and the word address bytes are transmitted to the TD24C64-C1 as part of the dummy write sequence (see **Figure 5–9**). Once the device address byte and word address bytes are clocked in and acknowledged by the TD24C64-C1, the Master must generate another Start condition. The Master initiates a Current Address Read by sending another device address byte with the R/$\overline{W}$ bit set to Logic 1. The TD24C64-C1 responds with an ACK to the device address byte and serially clocks out the first data word and

increments its internal address counter. The device will continue to transmit sequential data words as long as the Master continues to acknowledge each data word. To end the sequence, the Master responds with a NACK followed by a Stop condition.

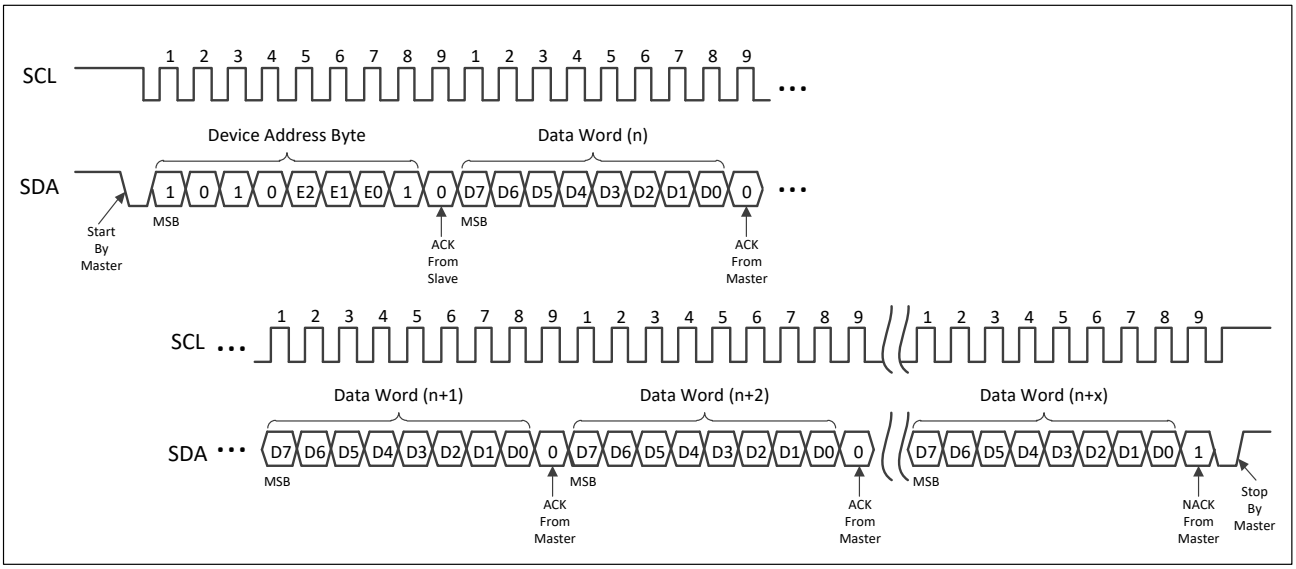
Figure 5–9 Random Read



5.2.3 Sequential Read

A Sequential Read operation is initiated in the same way as either a Current Address Read or a Random Read, except that after the TD24C64-C1 transmitting the first data word, the Master responds with an ACK instead of a NACK. As long as the TD24C64-C1 receives an ACK, it will continue to increment the data word address and serially clock out the sequential data words (see **Figure 5–10**). When the internal address counter is at the last byte of the last page, the word address will roll over to the beginning of the memory array and the Sequential Read operation will continue. The Sequential Read operation is terminated by the Master responding with a NACK followed by a Stop condition.

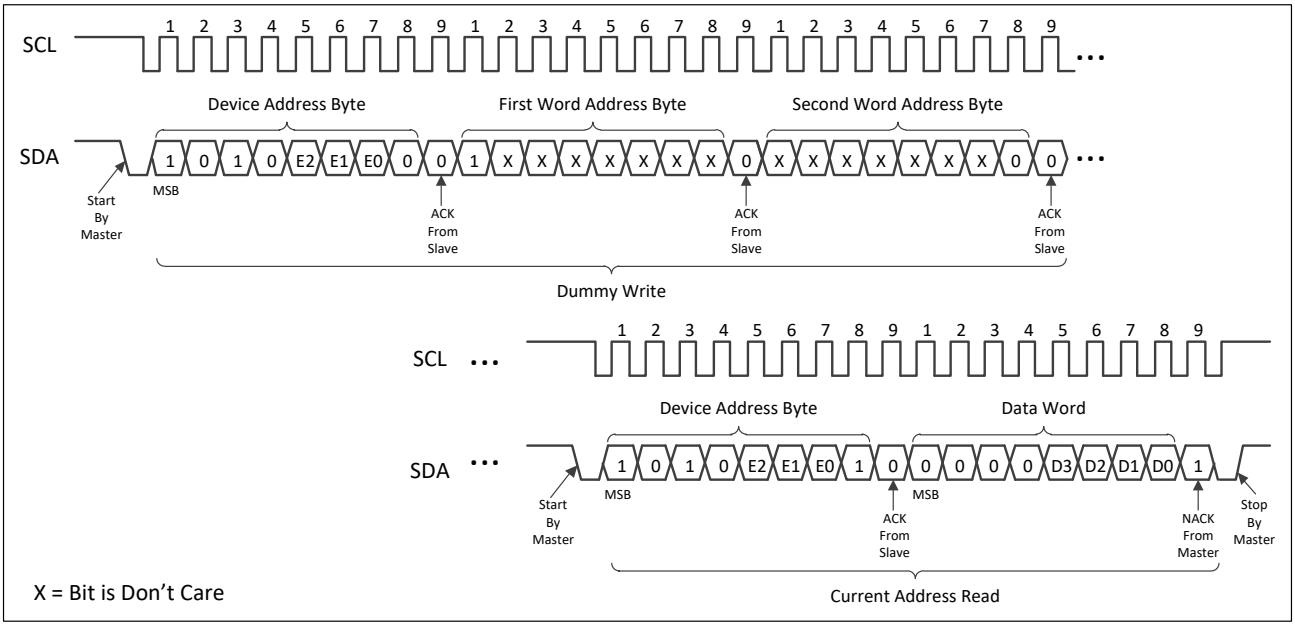
Figure 5–10 Sequential Read



5.2.4 Read Chip Enable Register

Reading the Chip Enable register is performed with a Random Read at address 1xxx_xxxx_xxxx_xxx0b (where 'x' is Don't Care). The higher four bits of the Chip Enable register content are read as '0000' (see **Figure 5–11**). The lower four bits (bit 3, bit 2, bit 1, and bit 0) are defined in **Section 3.1**. Reading more than one byte will loop on reading the Chip Enable register value.

Figure 5–11 Read Chip Enable Register



5.2.5 Read Identification Page

The Identification Page can be read by issuing a Read Identification Page instruction. This instruction uses the same protocol and format as Random Read, except that:

- The device type identifier is defined as '1011';
- The word address bits A10:A9 must be '00', bits A15:A11 and A8:A5 are Don't Care;
- The word address bits A4:A0 define the byte locations inside the ID Page (see **Table 4–3**).

When the end of Identification Page is reached, the word address will roll over to the beginning of the Identification Page. The Read Identification Page operation is terminated by the Master responding with a NACK followed by a Stop condition (see **Figure 5–12**).

5.2.6 Read Lock Status

The locked/unlocked status of the Identification Page can be checked by transmitting a specific truncated command, Write Identification Page instruction and one data byte, to the device. The device responds with an ACK to the data byte if the Identification Page is unlocked, or responds with a NACK if the Identification Page has been locked. Right after this, it is recommended to transmit a Start condition to the device followed by a Stop condition (see **Figure 5–13**), so that the truncated Write command will not be executed because the Start condition resets the device internal logic, and the device is then set back into Standby mode by the Stop condition.

Figure 5–12 Read Identification Page

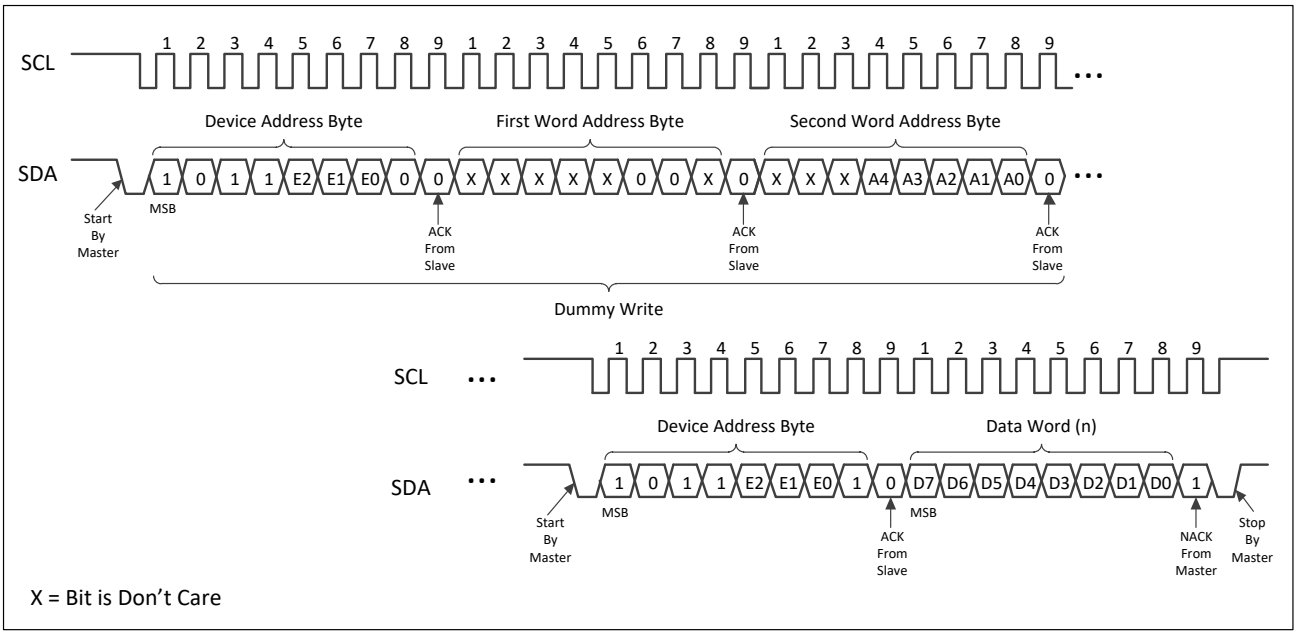
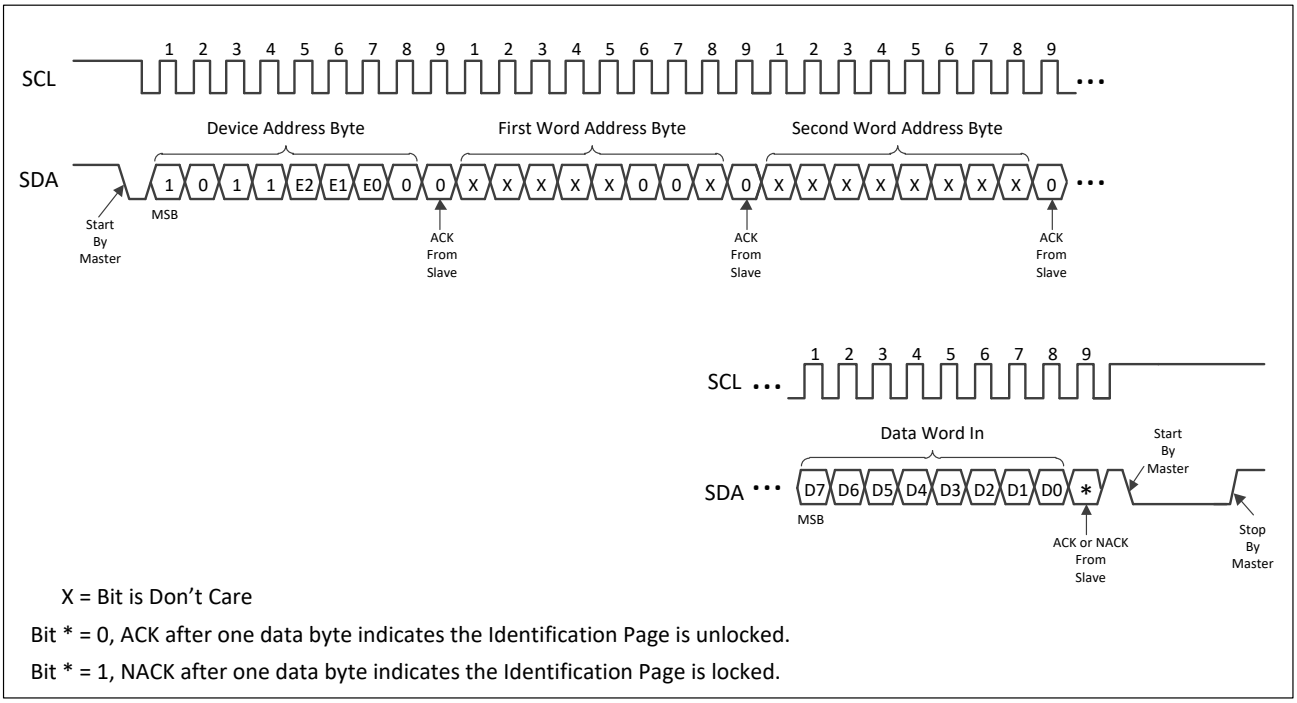


Figure 5–13 Read Lock Status of Identification Page



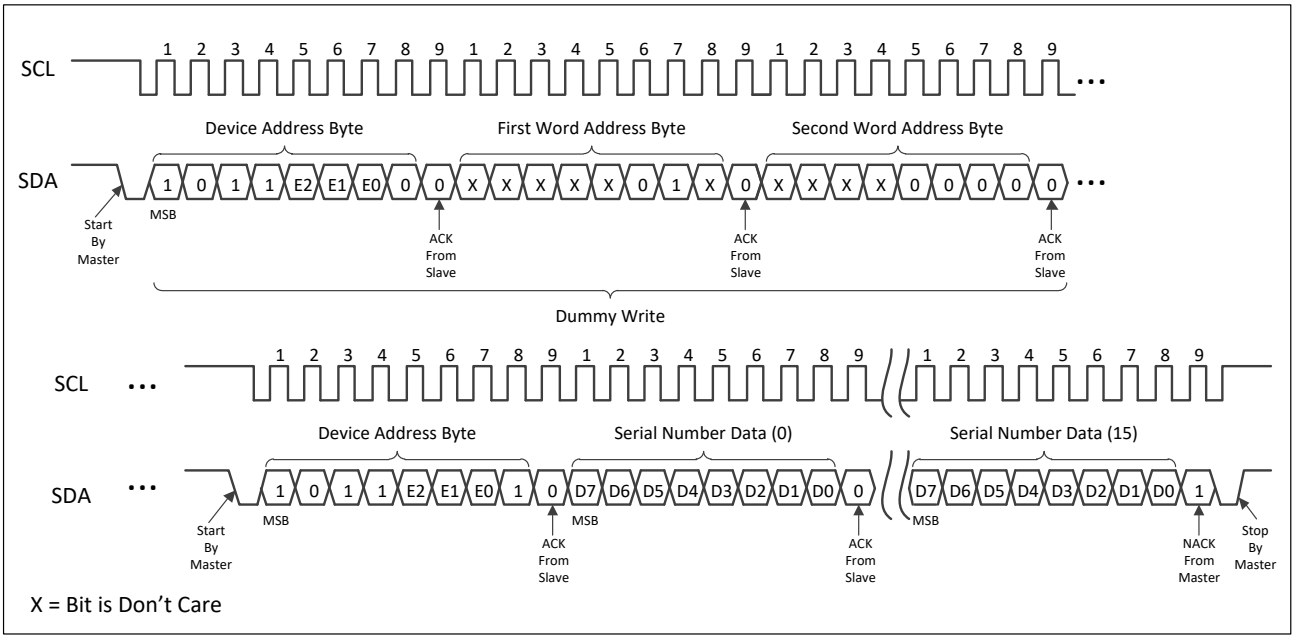
5.2.7 Read Unique ID

The TD24C64-C1 offers a separate memory block containing a factory programmed 128-bit Unique ID (UID), or Serial Number. Reading the Serial Number is similar to Sequential Read, except that:

- The device type identifier is defined as ‘1011’;
- The word address bits A10:A9 must be ‘01’, bits A15:A11 and A8:A4 are Don't Care;
- The word address bits A3:A0 define the byte locations inside the Unique ID (see **Table 4–3**).

In order to guarantee a unique number, the entire 128-bit value must be read from the starting address of the Serial Number block. To read the first byte of the Serial Number, the word address bits A3:A0 need to be ‘0000’. Writing or altering the 128-bit Unique ID is not allowed. When the end of the 128-bit UID block is reached (16 bytes of data), the word address will roll over to the beginning of the 128-bit UID block. The Read Unique ID operation is terminated when the Master responds with a NACK to the data byte followed by a Stop condition (see **Figure 5–14**).

Figure 5–14 Read Unique ID



6 Electrical Specifications

6.1 Absolute Maximum Ratings

Table 6–1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
	Ambient temperature with power applied	-55 to +130	°C
T_{STG}	Storage temperature	-65 to +150	°C
V_{CC}	Supply voltage	-0.5 to +6.5	V
V_{IN}	Voltage on input Pins	-0.5 to +6.5	V
V_{ESD}	Electrostatic pulse (human body model)	6000	V

Note: Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. Functional operation of the device at these ratings or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2 DC Characteristics

Operating range: T_A = -40°C to +105°C, V_{CC} = 1.7V to 5.5V (unless otherwise noted).

Table 6–2 DC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{CC}	Supply Voltage		1.7	5.5	V
I_{CC1}	Supply Current (Read)	V_{CC}= 1.7V, Read at 1MHz	-	0.1	mA
		V_{CC}= 1.8V, Read at 400 kHz	-	0.1	mA
		V_{CC}= 5.5V, Read at 400 kHz	-	0.4	mA
		V_{CC}= 5.5V, Read at 1MHz	-	0.5	mA
I_{CC2}	Supply Current (Write)	V_{CC}= 1.8V, Write at 400 kHz	-	0.2	mA
		V_{CC}= 5.5V, Write at 400 kHz	-	0.5	mA
I_{SB}	Standby Current	V_{CC} = 1.7V, V_{IN} = V_{CC} or V_{SS}	-	0.5	μA
		V_{CC} = 5.5V, V_{IN} = V_{CC} or V_{SS}	-	1.0	μA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}	-	1.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}	-	1.0	μA
V_{IL}	Input Low-Level Voltage (SDA, SCL)		-0.5	0.3*V_{CC}	V
V_{IH}	Input High-Level Voltage (SDA, SCL)		0.7*V_{CC}	V_{CC}+0.5	V
V_{OL1}	Low-Level Output Voltage	V_{CC}> 2V, I_{OL}= 3mA	-	0.4	V
V_{OL2}	Low-Level Output Voltage	V_{CC}≤2V, I_{OL}= 2mA	-	0.2	V

6.3 AC Characteristics

Operating range: T_A = -40°C to +105°C, V_{CC} = 1.7V to 5.5V, C_L = 100pF (unless otherwise noted).

Measurement conditions: Input rise and fall time ≤ 50ns

Input pulse voltages: 0.2*V_{CC} to 0.8*V_{CC}

Input and output timing reference voltages: 0.3*V_{CC} to 0.7*V_{CC}

Table 6–3 AC Characteristics

Symbol	Parameter	Fast V_{CC} = 1.7V to 5.5V		High Speed V_{CC} = 1.7V to 5.5V		Unit
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL	-	400	-	1000	kHz
t_{LOW}	Clock Pulse Width Low	1300	-	600	-	ns
t_{HIGH}	Clock Pulse Width High	600	-	260	-	ns
t_R[1]	SDA Rise Time	-	300	-	300	ns
t_F[1]	SDA(Out) Fall Time	-	300	-	100	ns
$t_{HD.STA}$	Start Hold Time	600	-	250	-	ns
$t_{SU.STA}$	Start Setup Time	600	-	250	-	ns
$t_{SU.STO}$	Stop Setup Time	600	-	250	-	ns
t_{BUF}	Bus Free Time between Stop and Next Start	1300	-	500	-	ns
$t_{HD.DI}$	Data In Hold Time	0.0	-	0.0	-	ns
$t_{SU.DAT}$	Data In Setup Time	100	-	50	-	ns
$t_{HD.DAT}$	Data Out Hold Time	50	-	50	-	ns
t_{AA}	SCL Low to Data Out Valid	100	900	50	500	ns
t_{WR}	Write Cycle Time	-	3	-	3	ms
t_I	Noise Suppression Time	-	50	-	50	ns

Note: [1] This parameter is ensured by characterization only.

Figure 6–1 Bus Timing

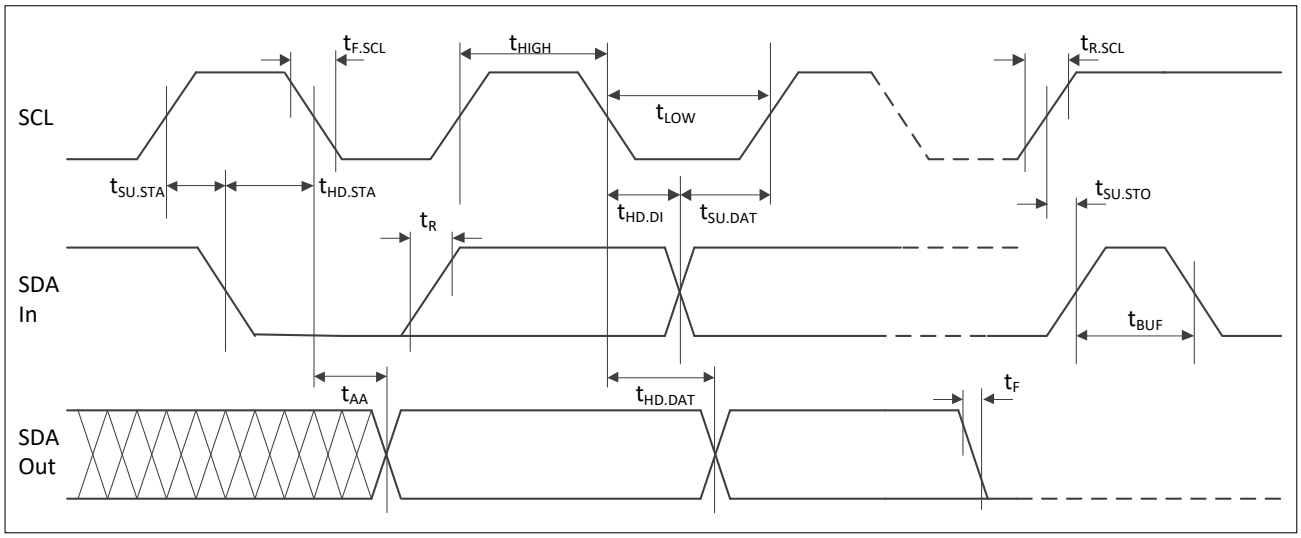
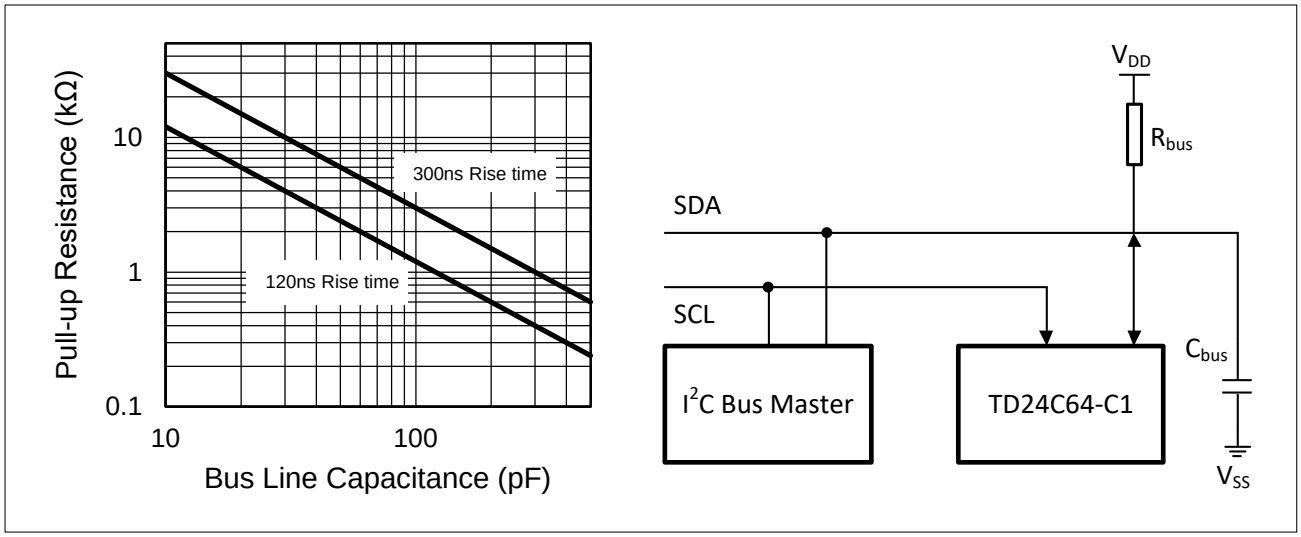


Figure 6–2 Maximum Pull-up Resistance vs. Bus Parasitic Capacitance



6.4 Pin Capacitance

Operating range for pin capacitance: T_A = +25°C, f_C = 1MHz, V_{CC} = 1.7V to 5.5V.

Table 6–4 Pin Capacitance

Symbol	Parameter[1]	Max	Unit	Test Condition
$C_{I/O}$	Input/output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

Note: [1] These parameters are ensured by characterization only.

6.5 Reliability Characteristics

Table 6–5 Reliability Characteristics

Symbol	Parameter	Min	Unit	Test Condition
N_W	Write Cycle Endurance	$2x10^6$	cycle	T_A = +25°C, Page Mode
D_R	Data Retention	200	year	T_A = +25°C

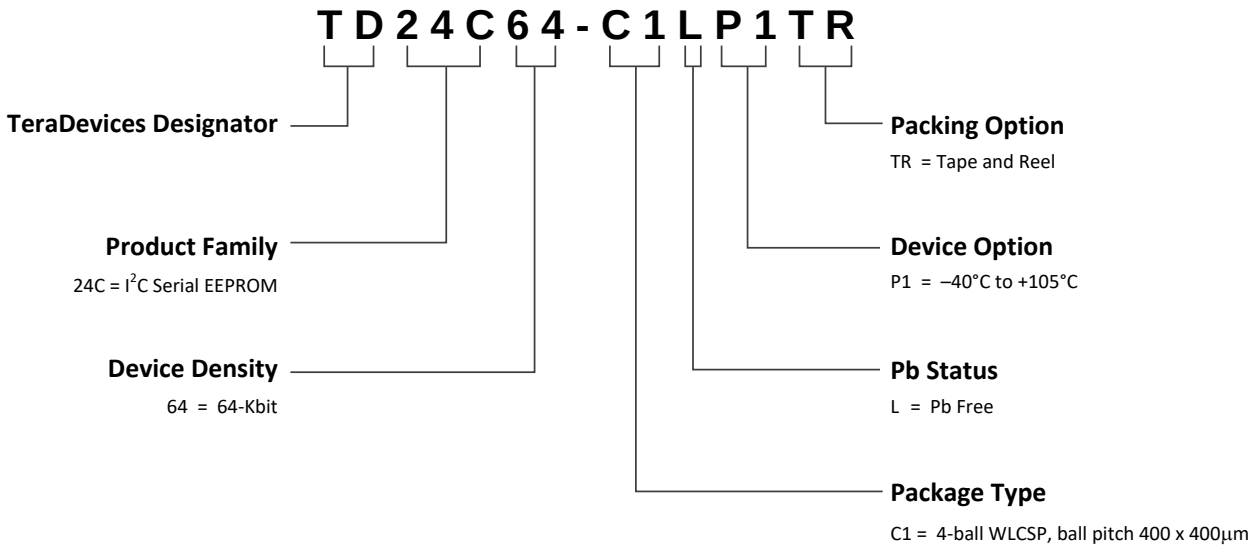
7 Initial Delivery State

The TD24C64-C1 serial EEPROM is delivered as follows:

- All bits in the memory array are set to ‘1’ (each byte contains FFh).
- All bits in the Chip Enable register are set to ‘0’ (00h).
- All bits in the Identification Page are set to ‘1’ (each byte contains FFh).

8 Ordering Information

Table 8–1 Ordering information scheme

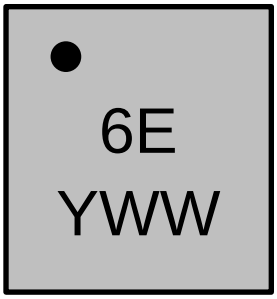


Package types not listed below may be available for order. Please contact TeraDevices for availability details.

Part Number	Package	Delivery Information	Temperature Range
TD24C64-C1LP1TR	4-ball WLCSP, ball pitch 400 x 400µm	Tape and Reel, 4000 units per Reel	-40°C to +105°C

9 Top Marking

9.1 WLCSP Package Marking



6E: TD24C64-C1LP1TR

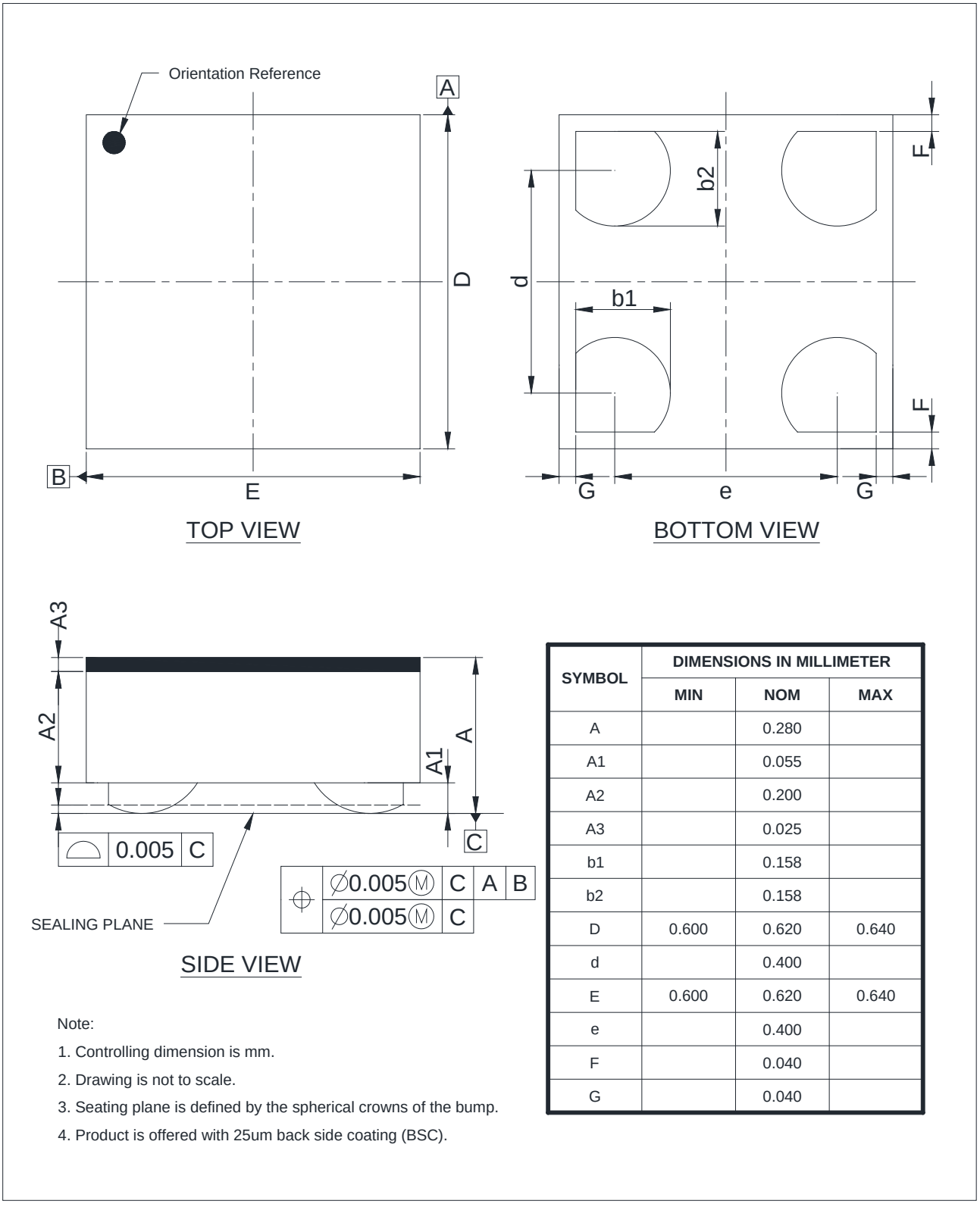
YWW: Date Code, Y = year, WW = week

Example: 040 = year 2020, week 40

10 Package Information

10.1 WLCSP Package Information

Figure 10–1 4-ball 400 x 400μm WLCSP Package Outline



SYMBOL	DIMENSIONS IN MILLIMETER		
	MIN	NOM	MAX
A		0.280	
A1		0.055	
A2		0.200	
A3		0.025	
b1		0.158	
b2		0.158	
D	0.600	0.620	0.640
d		0.400	
E	0.600	0.620	0.640
e		0.400	
F		0.040	
G		0.040	

Note:

1. Controlling dimension is mm.
2. Drawing is not to scale.
3. Seating plane is defined by the spherical crowns of the bump.
4. Product is offered with 25um back side coating (BSC).

11 Revision History

Revision	Date	Comments
Rev.1.0	Nov. 2020	Initial version release
Rev.1.1	Jul. 2021	Updated: — *Features* — description of bit 3, bit 2 and bit 1 in *Table 3–1* — V_{BOR} and t_{INIT} value in *Table 4–1* — I_{CC2} value in *Table 6–2*
Rev.1.2	Jul. 2022	Added: — notes for bit 3, bit 2 and bit 1 in *Table 3–1*